Switching loss reduction technique in active power filters without auxiliary circuits

Chi-Seng Lam[1,2], Man-Chung Wong[1,2], Ning-Yi Dai[2], Wai-Hei Choi[2], Xiao-Xi Cui[2], Chi-Yung Chung[3]

1 - *State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China*

2 - *Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao, China*

3 - *Department of Electrical and Computer Engineering, University of Saskatchewan, Saskatoon, Saskatchewan, Canada*

E-mail: cslam@umac.mo / c.s.lam@ieee.org

Abstract – In order to reduce the active power filter (APF) system switching loss, the usual method is to apply different soft-switching techniques. However, this would increase the system initial cost. In this paper, a switching loss and switching noise reduction control strategy for active power filter (APF) under reactive power and current harmonics compensation is proposed, which can be applied to the existing APF systems in worldwide, thus causing economical benefits. The minimum dc-link operating voltage of APF is computed through both fundamental and harmonic frequencies analysis. Then an adaptive dc-link voltage controller for the APF is proposed, such that the compensating range of the APF is adaptively varied according to the variation of the loading. Thus the switching loss and switching noise of the APF can be lowered. Moreover, the design criteria of the proportional and integral gains of the adaptive dc voltage controller are presented and discussed. Finally, simulation and experimental results of a 110V, 5kVA APF experimental prototype are given to prove the validity of the proposed control strategy for the APF in current quality compensation, and at the same time reducing switching loss and switching noise during operation.

Keywords – Adaptive dc-link voltage control, active power filters, current harmonics, reactive power, switching loss, switching noise.

1 Introduction

Traditionally, passive power filters (PPFs) have been considered as a good solution for current harmonics compensation and displacement power factor correction in distributed power systems [1–6] owing to their simplicity, low initial cost, etc. However, they have low dynamic performance, resonance problems, poor system robustness, etc. [1–6], in which those disadvantages are not appreciated for customers. Active Power Filter concept was firstly proposed by L. Gyugyi in 1976 [2], then the active power filters (APFs) were

rapidly developed since then. APFs can solve those problems existing in PPFs, but they have high rating with high initial cost limitation. Moreover, they need to bear a relative high switching loss and switching noise during operation. Conventionally, all APFs are being operated at a high constant dc-link voltage level for ensuring the compensation performance [1, 3–11]. In addition, as many APFs have been installed and are operating in Japan and all around the world [12], [13], their operating switching loss is a notable application concern. For example, the presented APF operating switching loss is about 7~9% at its 60% rated power [14] and 3~5% at its full rated power [15–17], which is a significant power loss. In order to reduce the APF system switching loss, the usual method is to apply soft-switching techniques. Table 1 summarizes the comparison among different soft-switching circuits [18–20]: actively clamped resonant dc-link (ACRDCL) [19], auxiliary resonant commutated pole (ARCP) [19, 20], and negative-bus auxiliary resonant circuit (NBARC) [18]. From Table 1, even though they can significantly reduce the APF inverter power loss, it is obvious that applying soft-switching techniques would increase the APF system initial cost because it requires extra switching devices, passive elements, etc. In order to increase the value proposition of the APF without changing its structure or design [21], it would be a good approach if its switching loss can be reduced by further develops the control algorithm for the existing APF systems. As the switching loss is directly proportional to the inverter voltage in dc side [22], a higher switching loss will be induced when the APF is being operated at a high dc-link voltage, and vice versa. Therefore, if the dc-link voltage can be varied according to different loading situations, the APF can obtain better performances and also reduce switching loss. However, the adaptive dc voltage control strategy for APF is still lack of investigation and study.

Table 1 Comparison among different soft-switching circuits [18–20]

Auxiliary circuit items	ACRDCL	ARCP	NBARC
No. of switches	1	6	2
No. of diode	1	6	2
No. of capacitor	2	6	1
No. of inductor	1	3	1
Peak voltage	1.5 ~ 1.8 p.u.	0.5 p.u.	0.5 & 1p.u.
Conducting losses	High	Low	Low
Insertion & resonant bus point	Positive dc-link	Positive dc-link	Negative dc-link
Inverter loss reduction (compared with hard-switching)	Maximum: ~ 60% at 10kHz, V_{dc}=300V, I_o=100A_{peak} [19]	Maximum: ~ 40% at18kHz, V_{dc}=300V, I_o=100A_{peak} [19]	--- [18] (power device temp. ↓ by 15% & 11% at 50% & 100% loading to reflect loss ↓)

In [23], parameter design procedures for minimum dc-link voltage operation of hybrid power quality compensator (HPQC) in high speed co-phase traction power supply system are proposed. The HPQC is composed of two single-phase converters with connected back-to-back and sharing the same dc-link capacitor for energy exchange. One of the converters is connected to two phases of the three-phase power system through coupling inductors (L coupling) and single phase V/V transformer, while the other one is connected to them through coupling capacitor and inductor (LC coupling) and single-phase V/V transformer. However, this work does not present any dc-link voltage control strategy for HPQC and just provides an extra dc voltage source for perform simulations and experiments. To reduce the switching loss and switching noise for the HAPF, the authors in [24] proposed an adaptive dc-link voltage control strategy for three-phase HAPF reactive power compensation only, but the proposed strategy does not include current harmonic consideration. In [25], the minimum dc-link voltage deduction for HAPF without and with coupling neutral inductor is proposed, and the advantages of adding neutral inductor are also discussed. However, the dc voltage control strategy is not being discussed in [25]. Based on the works presented in [24] and [25], the authors in [26] develop and integrate the adaptive dc voltage control strategy [24] and the addition of coupling neutral inductor [25] into the HAPF in both dynamic reactive power and current harmonics compensation, in which the switching loss and switching noise can be greatly reduced. After the development of adaptive dc voltage control for HAPF [24–26], it proves that the adaptive control strategy can bring benefits (switching loss and switching noise reduction) to the HAPF system during operation. In this paper, based on the effective results in [27], the adaptive dc voltage control idea is migrated into the APF to investigate its switching loss and switching noise reduction performances. So that this adaptive dc control strategy can also be applied to the existing APF systems in worldwide, thus causing some economical benefits.

Even though the adaptive dc voltage control strategy has been proposed in HAPF, the control algorithm cannot be simply and directly applied into APF. Therefore, it is necessary to do further research analysis and investigation, which is the motivation of this paper. Furthermore, the main contributions of this paper are:

- Deduce and analyze APF minimum dc-link voltage for reactive power and current harmonics compensation with the help of reference [27];
- Propose an adaptive dc-link voltage control strategy for APF reducing switching loss and noise, and improve compensation performance;
- Present and analyze the design criteria of the proportional and integral gains of the dc-link voltage controller;
- Present extensive simulation and experimental results for an 110V, 5kVA APF experimental prototype to validate the proposed control technique in comparison to the conventional method.

In this paper, a brief introduction of research background and motivation is covered in section 1. In section 2, a three-phase four-wire APF with its corresponding equivalent fundamental and harmonic circuit models are presented. According to its circuit models, the required minimum dc-link voltage can be calculated. Then the adaptive dc-link voltage controller for the APF and also the design criteria of its proportional and integral gains are presented and discussed in section 3. In section 4, the parameters selection of the APF system, simulation verifications and experimental results obtained from hardware prototype are presented. Finally, a conclusion is given in section 5. As this paper mainly focuses on the APF application in low voltage power distribution side, the neutral wire usually presents and the following analysis and discussion will only focus on inductive loads.

2 A three-phase four-wire APF required minimum dc-link voltage for reactive power and current harmonics compensation

The overall circuit diagram of the three-phase four-wire active power filter (APF) is illustrated in Fig. 1, where the subscript 'x' represents phase a,b,c,n. v_{sx} represents the source voltage, v_x represents the load voltage, L_s represents the system inductance. i_{sx}, i_{Lx} and i_{cx} represent the source, load and inverter current. L_c represents the coupling inductor. C_{dc} is dc-link capacitor and the upper and lower dc capacitor voltages are represented by V_{dcU} and V_{dcL} with V_{dcU}=V_{dcL}=0.5V_{dc}.

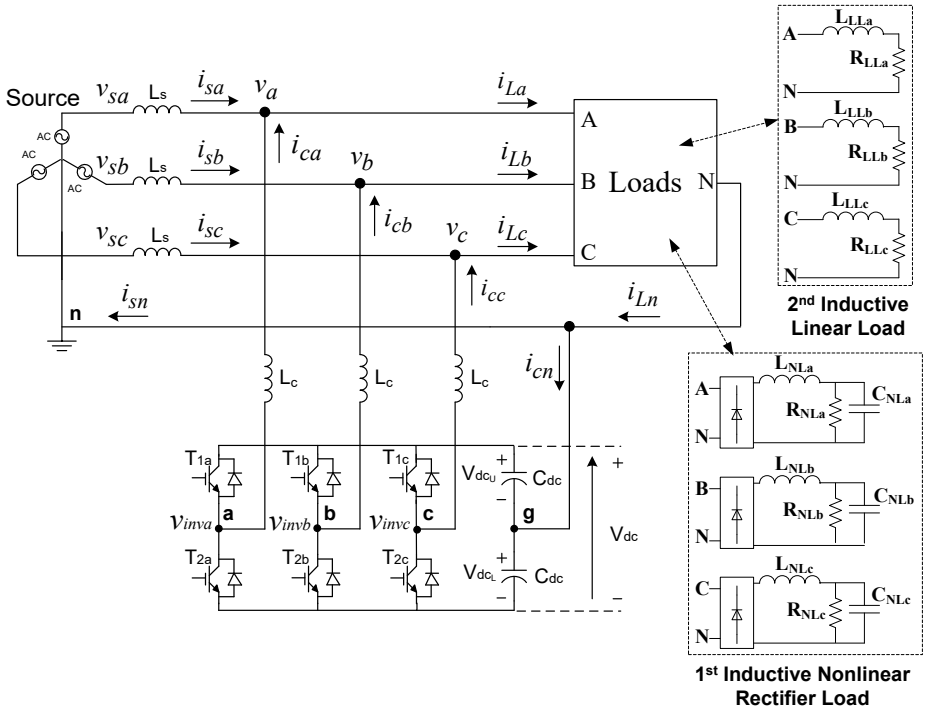


Fig. 1. Circuit structure of a three-phase four-wire APF.

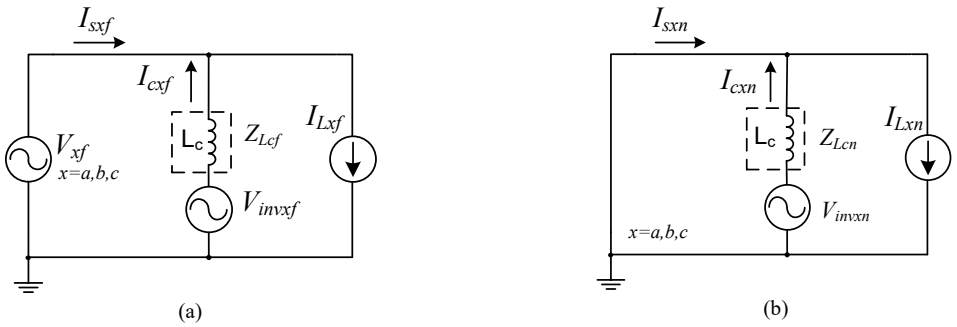


Fig. 2. APF equivalent single-phase circuit models at: (a) fundamental frequency, (b) harmonic frequency.

The APF equivalent single-phase circuit models at fundamental and harmonic frequency are shown in Fig. 2, where the subscripts '*f*' and '*n*' represent the fundamental and harmonic frequency components. And the active part of APF can be regarded as a controllable voltage source by pulse-width modulation (PWM) technique. All parameters for the following analysis are in root mean square (rms) values.

2.1 Required dc-link voltage at fundamental frequency

If v_{sx} and v_x as shown in Fig. 1 are pure sinusoidal without harmonic components, $\vec{V}_{sx} = \vec{V}_x = \vec{V}_{xf} = \left|\vec{V}_x\right| = V_x$. From Fig. 2(a), the voltage vector of APF inverter at fundamental frequency is expressed as: :

$$\vec{V}_{invx_f} = \vec{V}_x + \vec{Z}_{Lc_f} \cdot \vec{I}_{cx_f} \tag{1}$$

All vectors in (1) are in fundamental frequency, where the compensating current $\vec{I}_{cx_f}$ is composed by $\vec{I}_{cx_f} = I_{cx_{fp}} + jI_{cx_{fq}}$. The subscripts '*p*' and '*q*' represent the active and reactive components respectively. I_{cxfp} represents the fundamental active current for contributing the active power flow between the source and APF while I_{cxfq} represents the fundamental reactive current for compensating loading reactive power. $\vec{V}_{invx_f}$ in (1) can also be rewritten as:

$$\vec{V}_{invx_f} = V_{invx_{fp}} + jV_{invx_{fq}} \tag{2}$$

$$\text{where} \quad \begin{aligned} V_{invx_{fp}} &= V_x - I_{cx_{fq}} X_{Lc_f} \\ V_{invx_{fq}} &= I_{cx_{fp}} X_{Lc_f} \end{aligned} \tag{3}$$

From (3), I_{cxfp} and I_{cxfq} can be expressed as:

$$I_{cx_{fp}} = \frac{V_{invx_{fq}}}{X_{Lc_f}} \tag{4}$$

$$I_{cx_{fq}} = \frac{V_x - V_{invx_{fp}}}{X_{Lc_f}} \tag{5}$$

On the condition that the inverter dc voltage control is implemented, the steady-state I_{cxfp} from the inverter is small ($I_{cxfp} \approx 0$). For $V_{dcU}=V_{dcL}=0.5V_{dc}$ and modulation index $m=1$, R_{Vdc} represents the ratio between V_{dcU}, V_{dcL} and load voltage V_x reference to neutral *n* [24]:

$$R_{V_{dc}} = \frac{\pm V_{invxf}}{V_x} = \frac{\pm 0.5V_{dc}/\sqrt{2}}{V_x} = \pm\frac{V_{dc}}{2\sqrt{2}\,V_x} \tag{6}$$

where V_{invxf} is the inverter fundamental voltage in rms value.

As the active fundamental current I_{cxfp} is assumed to be very small ($I_{cxfp} \approx 0$) at steady-state, the APF injects pure fundamental reactive current, the reactive power (Q_{cxf}) provided by the APF can be computed as:

$$Q_{cx_f} = Im(V_x I_{cx_f}{}^*) = -V_x I_{cx_{fq}} = -Q_{cx_{f\_Lc}}(1 - R_{V_{dc}}) \tag{7}$$

where $Q_{cx_{f\_Lc}} = \frac{V_x{}^2}{X_{Lc_f}} > 0$, which is the reactive power provided by the coupling inductor.

From Fig. 1, to achieve the source-side reactive power $Q_{sxf}=0$, the compensating reactive power should be equaled to the loading reactive power, i.e. $Q_{cxf} = Q_{Lxf}$. By setting $Q_{cxf} = Q_{Lxf}$, via (6) and (7), the required minimum dc voltage V_{dcxf} for reactive power compensation in each phase can be found:

$$V_{dcxf} = \sqrt{2} V_{invxf} = \sqrt{2}\, V_x \cdot N \tag{8}$$

where $N = \left| 1 + \frac{Q_{Lx_f}}{Q_{cx_{f\_Lc}}} \right|$. Once Q_{Lxf} is calculated, V_{dcxf} in each phase can be obtained.

1) For pure resistive load consideration: When the load is pure resistive, the loading reactive power $Q_{Lxf}=0$, $N=1$. From (8), the required $V_{dcxf} = 2\sqrt{2}\, V_x$.

2) For inductive load consideration: When the load is inductive, $Q_{Lxf}>0$, $N>1$ as $Q_{cxf\_Lc}>0$. From (8), the required $V_{dcxf} = 2\sqrt{2}\, V_x \cdot N > 2\sqrt{2}\, V_x$.

3) For capacitive load consideration: When the load is capacitive, $Q_{Lxf}<0$, $N \in R$. Thus, the required $V_{dcxf} = 2\sqrt{2}\, V_x \cdot N$. When $Q_{Lxf} = -Q_{cxf\_Lc}$, the minimum dc-link voltage requirement (V_{dcxf} =0) can be achieved. Moreover, V_{dcxf} can be larger or smaller than $2\sqrt{2}\, V_x$, which depends on the sign of Q_{Lxf} and the values of Q_{Lxf} and Q_{cxf_Lc}.

2.2 Required dc-link voltage at harmonic frequency

To compensate harmonic current generated by the non-linear load, APF should provide the corresponding harmonic output voltages V_{invxn}. According to Fig. 2(b), V_{invxn} at each *nth* order current harmonic can be expressed as:

$$V_{invxn} = |n\omega L_c \| I_{cxn}| \qquad n = 2,3...\infty \tag{9}$$

where I_{cxn} represents the *nth* order compensating current. When the APF is used to perform current harmonic compensation, the absolute I_{cxn} should be equal to:

$$|I_{cxn}| = |I_{Lxn}| \tag{10}$$

where I_{Lxn} is the *nth* order harmonic current of the loading. Thus, the required minimum dc-link voltage at each harmonic order V_{dcxn} for compensating the corresponding harmonic current can be found:

$$V_{dcxn} = \sqrt{2} V_{invxn} = \sqrt{2}\, |n\omega L_c \| I_{cxn}| \tag{11}$$

In the following, the APF final required dc-link voltage for both reactive power and current harmonics compensation will be presented and discussed.

2.3 Final required dc-link voltage

Combining the required dc-link voltage in both fundamental and harmonic circuits, the final dc-link voltage V_{dcx} can be computed by taking their rms value, thus, V_{dcx} can be expressed as:

$$V_{dcx} = \sqrt{\left|V_{dcxf}\right|^2 + \sum_{n=2}^{\infty} \left|V_{dcxn}\right|^2} \tag{12}$$

Assumed that there are slight deviations among three-phase compensating currents of APF, thus there are three sets of minimum dc-link voltage value with respect to each phase parameter values. In order to guarantee the compensation performance of APF in each phase, the final required minimum dc-link voltage (V_{dc_min}) for the three-phase four-wire APF can be obtained by (13), where the calculated value by (13) is sufficient to compensate the reactive power and current harmonics problems for three phases. Table 2 summarizes the minimum dc-link voltage deduction steps of the three-phase four-wire APF, in which it has different V_{dcxf} and V_{dcxn} equations as compared with those of HAPF [24 – 26].

$$V_{dc\_min} = \max(2V_{dca}, 2V_{dcb}, 2V_{dcc}) \tag{13}$$

Table 2 Minimum dc-link voltage deduction steps of the APF

1) Fundamental Frequency	Minimum dc-link voltage for compensating reactive power: $V_{dcxf} = \sqrt{2}\, V_{invxf} = \sqrt{2}\, V_x \left| 1 + \frac{Q_{Lx_f}}{\left|Q_{cx_{f\_Lc}}\right|} \right|$ (8) where Q_{Lxf} is loading fundamental reactive power, Q_{cxf_Lc} is the reactive power provided by coupling L_c.
2) Harmonic Frequencies	Minimum dc-link voltage for compensating each *nth* order current harmonic: $V_{dcxn} = \sqrt{2} V_{invxn} = \sqrt{2} \left| n\omega L_c \right\| I_{cxn} \right|$ (11) where $\left|I_{cxn}\right| = \left|I_{Lxn}\right|$, $n=2, 3 \ldots \infty$, $\omega = 2\pi f$
3) All Frequencies	Minimum dc-link voltage: $V_{dc\_min} = \max(2V_{dca}, 2V_{dcb}, 2V_{dcc})$ (13) Where $V_{dcx} = \sqrt{\left|V_{dcxf}\right|^2 + \sum_{n=2}^{\infty} \left|V_{dcxn}\right|^2}$ (12) where $n=2, 3 \ldots \infty$

3 Adaptive dc-link voltage control strategy for a three-phase four-wire APF

In the following, the adaptive dc-link voltage control strategy is being applied to the three-phase four-wire APF system for lowering the operational switching loss and switching noise. The overall control block diagram is shown in Fig. 3, in which it consists of the following control blocks.

3.1 Instantaneous power compensation control block

The reference compensating currents for APF (i_{cx_q}) are calculated by the three-phase instantaneous *pq* theory [28].

3.2 Adaptive dc-link voltage control block

The adaptive dc-link voltage control block is composed by three control algorithms: 1) computation of adaptive minimum dc-link voltage V_{dc_min}, 2) determination of final reference dc-link voltage level V_{dc}^* and 3) P/PI control for dc-link voltage tracking.

1) Computation of adaptive minimum dc-link voltage (V_{dc_min}): First of all, the loading instantaneous reactive power q_{Lxf} is obtained with the help of single-phase instantaneous *pq* theory [29] and low-pass filters with cut-off frequency f_{cut}=5Hz . As $-q_{Lxf}/2$ can usually keep as a constant value for one cycle or more, the loading fundamental reactive power consumption Q_{Lxf} in each phase can be approximately treated as $Q_{Lxf} \approx -q_{Lxf}/2$. The required V_{dcxf} for compensating each phase Q_{Lxf} can be calculated by using (8). By using Fast Fourier Transform (FFT), the load current spectra $|I_{Lxn}|$ up to the considered harmonic order *n* can be computed. Then the required V_{dcxn} for compensating each *nth* order harmonic can be calculated by using (11). Finally, V_{dc_min} for the three-phase four-wire APF can be determined by (12) and (13).

2) Determination of final reference dc-link voltage level (V_{dc}^*): The adaptive dc control strategy will vary the reference V_{dc}^* in reality, thus may cause a frequent dc voltage fluctuation, and deteriorate the APF performances [30]. To relax this, V_{dc}^* determination process proposed in [24] is applied.

3) P/PI control for dc-link voltage tracking: The adaptive dc voltage level for APF can be achieved by feedback dc voltage controlled signal as active current reference component (dc_p) instead of both active and reactive current reference components of HAPF [24, 26, 31], the phenomenon can be explained with the help of [31]:

$$dc_p = K_p \cdot (V_{dc}^* - V_{dc}) + K_I \int (V_{dc}^* - V_{dc})dt \tag{14}$$

where dc_p aims to change and maintain the dc-link voltage level. K_p is the proportional gain, while K_I is the integral gain of the controller. With the help of the three-phase instantaneous *pq* theory [28] and dc_p term, V_{dc} can track its reference V_{dc}^* by varying the three-phase dc voltage control reference compensating

currents i_{cx_dc} in *a-b-c* coordinates. In the following, the design criteria for K_p and K_I will be discussed.

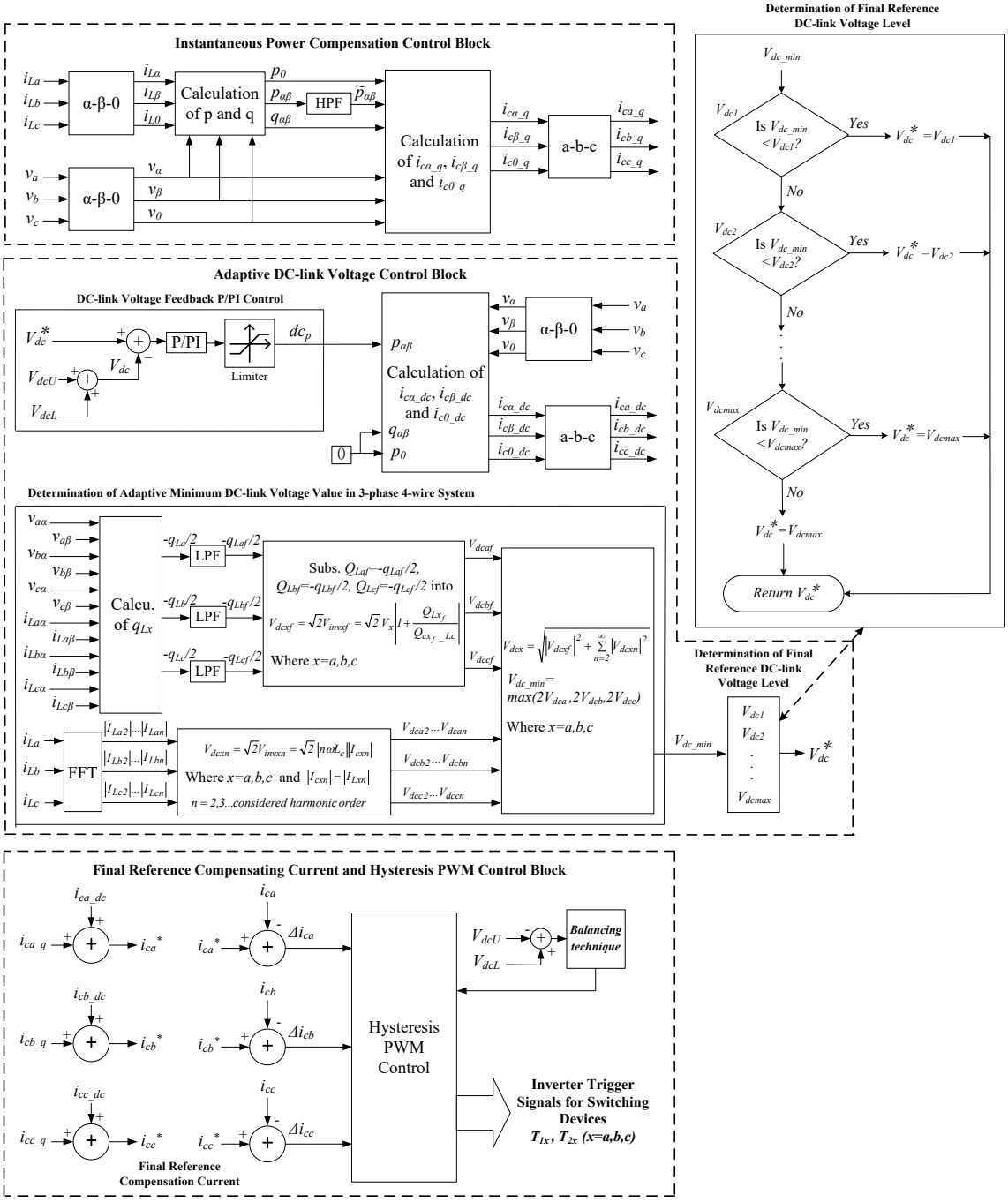


Fig. 3. Adaptive dc-link voltage control block diagram for APF.

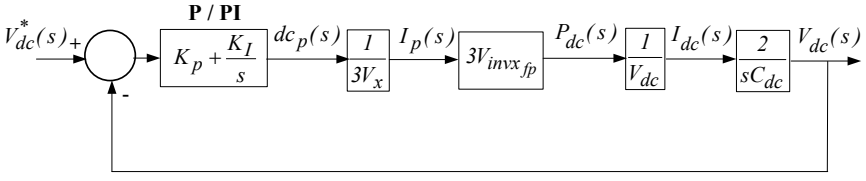


Fig. 4. Block diagram of APF dc-link voltage control.

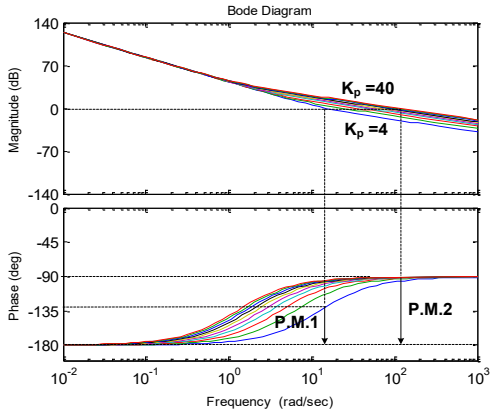
Fig. 4 shows the dc-link voltage control block diagram of APF, where $V_{invxfp} = |V_x + |I_{cxfq}| |X_{Lcf}||$ is the active

component of inverter fundamental voltage, I_{cxfq} is fundamental reactive compensating current. When PI controller is applied, the close-loop transfer function can be expressed as:

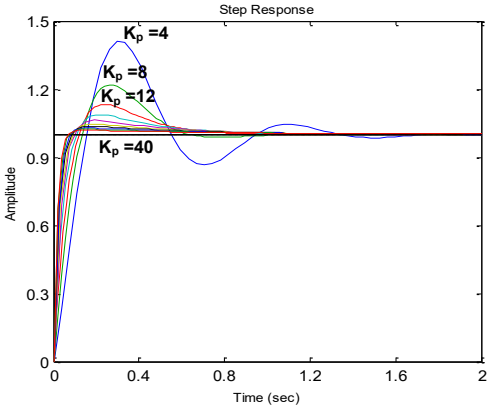
$$\frac{V_{dc}(s)}{V_{dc}^{*}(s)}=\frac{\frac{2V_{invxfp}K_p}{V_xV_{dc}C_{dc}}s+\frac{2V_{invxfp}K_I}{V_xV_{dc}C_{dc}}}{s^2+\frac{2V_{invxfp}K_p}{V_xV_{dc}C_{dc}}s+\frac{2V_{invxfp}K_I}{V_xV_{dc}C_{dc}}} \tag{15}$$

By ROUTH-HURWITZ criterion, the Routh table for (15) can be obtained. As K_p and $K_I>0$, the dc voltage controller is stable. From the APF system parameters in Table 3, L_c=30mH, C_{dc}=3.3mF and V_x=110V. For the dc-link maximum operating voltage is V_{dcU}, V_{dcL}=300V, the fundamental compensating reactive current is $|I_{cxfq}|$=4.8A, when K_I=50, the effect of K_p to the controller's stability and dynamic response are shown in Figs. 5(a) and (b). From Figs. 5(a) and (b), when K_p is varying from 4 to 40, the phase margins are increasing from P.M.1 to P.M.2, which can improve the controllers' stability. Moreover, a larger K_p value can also yield a faster dynamic response.

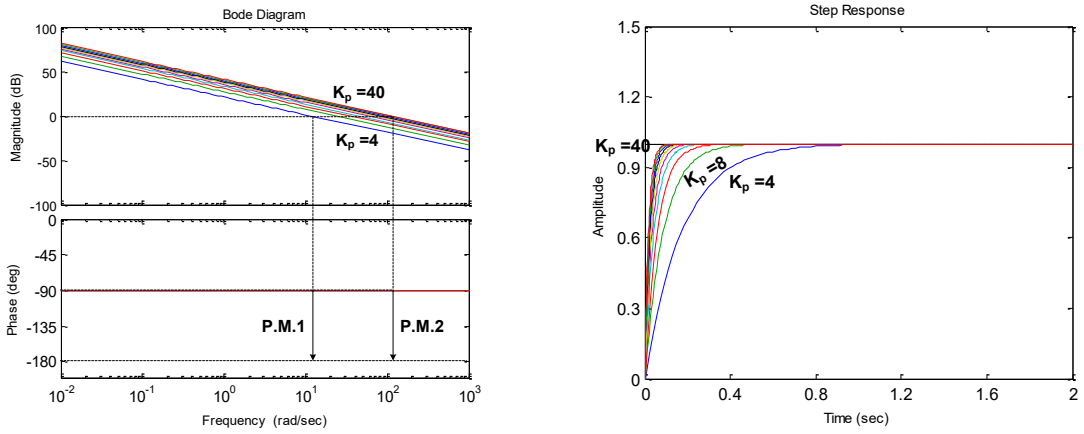
When only P controller is applied, that is K_I=0 in Fig. 4, the close-loop transfer functions can be deduced from (15). By Routh tables, as K_p>0, the controller is stable. If K_p is selected too large, it yields a large fluctuation at steady-state. On the other hand, if it is selected too small, a long settling time and a significant steady-state error will happen. In addition, the effect of K_p to the controller's stability and dynamic response are shown in Figs. 5(c) and (d). From Figs. 5(c) and (d), when K_p is varying from 4 to 40, their phase margins (P.M.1 and P.M.2) do not change at all, and the controller obtain good stability. Moreover, a larger K_p value can yield a faster dynamic response.



(a)



(b)



(c) (d)

Fig. 5. Stability and dynamic response of dc-link voltage feedback PI/P controller:
(a) bode diagram with PI controller when K_I=50 and K_p varies from 4 to 40,
(b) step response with PI controller when K_I=50 and K_p varies from 4 to 40,
(c) bode diagram with P controller when K_p varies from 4 to 40,
(d) step response with P controller when K_p varies from 4 to 40.

In this paper, P controller is chosen because of its simplicity and memory resource saving in the digital signal processor (DSP). If zero steady-state error of dc control is appreciated, PI controller can be chosen. A limiter is also implemented to prevent the controller's overflow problem.

From [28], the three-phase instantaneous load voltages (v_a, v_b, v_c) on the *a-b-c* coordinates can be transformed into those on the *α-β-0* coordinates by the Clarke transformation:

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{16}$$

The three-phase dc voltage control reference compensating currents in *α-β-0* coordinates can be calculated via (17):

$$\begin{bmatrix} i_{c0\_dc} \\ i_{c\alpha\_dc} \\ i_{c\beta\_dc} \end{bmatrix} = \frac{1}{v_{\alpha\beta}^2} \begin{bmatrix} v_{\alpha\beta}^2 & 0 & 0 \\ 0 & v_\alpha & -v_\beta \\ 0 & v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ dc_p \\ 0 \end{bmatrix} \tag{17}$$

where $v_{\alpha\beta}^2 = v_\alpha^2 + v_\beta^2$, dc_p can be determined by (14). Finally, the three-phase dc voltage control reference compensating currents i_{cx_dc} in *a-b-c* coordinates can be obtained by the inverse matrix of Clarke transformation in *α-β-0* coordinates, then V_{dc} can track V_{dc}^* by varying i_{cx_dc}.

$$\begin{bmatrix} i_{ca\_dc} \\ i_{cb\_dc} \\ i_{cc\_dc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{c0\_dc} \\ i_{c\alpha\_dc} \\ i_{c\beta\_dc} \end{bmatrix} \tag{18}$$

3.3 Final reference compensating current and hysteresis PWM control block

The hysteresis PWM [32] is applied for the PWM control part. After i_{cx_q} and i_{cx_dc} are calculated, the final reference compensating current $i_{cx}^{*} = i_{cx\_q} + i_{cx\_dc}$. After that, i_{cx}^{*} and i_{cx} will be sent to the hysteresis PWM control module for generating the corresponding PWM trigger signals to drive the power electronic switching devices. The dc capacitor voltage balancing concepts and techniques in [33] is also applied to balance the V_{dcU} and V_{dcL}.

4 Simulation and experimental results

Table 3 lists the system and APF parameters for simulations and experiments. As this paper mainly focuses on the APF application in low voltage power distribution side, from [34], the inductance for a low voltage distribution line is about 0.223mH/km and the length of a low voltage distribution line is usually no more than 1km, thus its equivalent impedance is usually less than 0.1mH. In addition, during the APF experimental testing in the laboratory, a small rating coupling transformer is used to reduce grid voltage from 230V to 110V. By considering them, the line inductance of the power distribution system of L_s =0.5mH is put in the simulation study in this paper. In practical case, an 11kV to 400V transformer is applied in the distribution system, and the rating compared to our experimental platform is much larger, thus the impedance is much smaller to reduce the voltage drop across it. As discussed before, V_{dc}^{*} is pre-set into certain voltage levels (V_{dcU}, V_{dcL} = 200V, 250V and 300V) for preventing inverter dc voltage fluctuation phenomenon under the adaptive dc voltage control strategy. To simplify the verification, the three-phase loadings are balanced as illustrated in Fig. 6.

Simulation were carried out by using PSCAD/EMTDC. An 110V, 5kVA three-phase four-wire APF experimental prototype is designed and constructed in the laboratory. The digital control system of the APF is a digital signal processor (DSP) TMS320F2812. Moreover, the Mitsubishi IGBT intelligent power modules PM300DSA60 are employed as the switching devices of the inverter, and their switching frequency limitation are at 20kHz. The sampling frequency of the control system is 25kHz in both simulation and experiment. The hysteresis current PWM [32] is applied to achieve the compensating current tracking in this paper, in which the switching frequency is not fixed. The maximum switching frequency is 12.5kHz, while

the average switching frequency is around 4kHz at fixed V_{dcU}, V_{dcL} =300V. From [35], it is suggested to select a coupling inductor L_c value close to the lower boundary because it could provide better current tracking speed with acceptable current ripples for APF. Thus, the coupling L_c of the APF can be designed via (19) [35], which is different from the design for HAPF based on one dominant current harmonic order [25, 26]:

$$L_c \geq \frac{V_{dc\,max}}{8 f_{sw} \Delta I_{ripple}} \tag{19}$$

where V_{dcmax} is the maximum dc-link voltage, ΔI_{ripple} is the maximum current ripple, f_{sw} is the switching frequency. For V_{dcmax}=600V, ΔI_{ripple}=0.8A and the average f_{sw} =4kHz, the coupling inductor L_c should be designed larger than 23.4mH. Therefore, L_c is chosen to be 30mH in this paper. In addition, this inductor value seems to be large because the capacity of the testing APF system in the laboratory is small compared with those APF systems in the market [15 – 17]. If the current rating (capacity) of the APF increases, that means the allowable ΔI_{ripple} is lager, the required coupling L_c can be chosen an appropriate small value accordingly (19), because the coupling L_c is inversely proportional to the current rating of the APF. In practical case, the capacity of the APF system is usually much larger than our experimental prototype, thus the coupling L_c for large capacity APF system will be usually much smaller than our case.

Table 3 System and APF parameters for simulations and experiments

System Parameters			Physical Values
System voltage and frequency		V_x, f	110V, 50Hz
System inductance		L_s	0.5mH
Coupling inductance		L_c	30mH
DC capacitor		C_{dc}	3.3mF
DC-link voltage levels		V_{dcU}, V_{dcL}	200V, 250V, 300V
1st inductive nonlinear loading	A,B,C	R_{NLx}, L_{NLx}, C_{NLx}	50.0Ω, 35.0mH, 400μF
2nd inductive linear loading	A,B,C	R_{LLx}, L_{LLx}	15.0Ω, 50.0mH

Table 4 APF minimum dc-link voltage levels (200V, 250V and 300V)

Different Situations:		Required $V_{dc\_min}/2$	Final Minimum Adapt. Level V_{dcU}, V_{dcL}
1st loading	A,B,C	176V	200V
1st & 2nd loadings	A,B,C	210V	250V

Fig. 6 show the simulated and experimental power factor (PF), total harmonic distortion (THD_{isx}) of i_{sx}

and system neutral current (i_{sn}) under different loading cases. When the 1st loading is connected, the three-phase simulated PF, THD_{isx} and i_{sn} are 0.77, 35.5% and 2.77A respectively, while the three-phase experimental PF =0.80, 0.80, 0.80, THD_{isx}= 33.1%, 32.5%, 32.3% and i_{sn} = 2.54A, respectively. When 1st and 2nd loadings are connected, the three-phase simulated PF, THD_{isx} and i_{sn} are 0.78, 13.8% and 2.86A respectively while the three-phase experimental PF =0.74, 0.79, 0.77, THD_{isx}= 11.7%, 12.5%, 12.2% and i_{sn} = 2.60A, respectively. Tables 5 and 8 illustrate the simulation and experimental results before APF compensation.

For the nonlinear rectifier load as shown in Fig. 1, the most dominant harmonic current orders are 3rd, 5th, 7th and 9th respectively. To simplify the dc-link voltage calculation process in this paper, the required dc-link voltage for current harmonics compensation is calculated up to 9th order only because the load harmonic current contents beyond 9th order are small. Of course, in general case, the required dc-link voltage can be calculated up to the considered load current harmonic order n. Refer to the pre-set voltage levels (V_{dcU}, V_{dcL} = 200V, 250V and 300V), from Table 4, the APF required minimum V_{dcU}, V_{dcL} = 200V and 250V for compensating the 1st loading and 1st and 2nd loadings. In addition, the power loss of APF can be calculated by measuring the collector-emitter voltage and current of each IGBT first, then the total inverter power loss P_{loss} can be found though the following equation (20) [36]:

$$P_{Loss} = \sum_{n=0}^{n=6} P_{Loss,n} = \sum_{n=0}^{n=6} \frac{1}{t_f} \int_0^{T_f} v_{ce,n}(t) \cdot i_{ce,n}(t) dt \tag{20}$$

where $v_{ce,n}(t)$ and $i_{ce,n}(t)$ are the collector-emitter voltage and current of IGBT respectively. t_f is a fundamental period and n is the number of IGBT. In the following, simulation and experimental results for the proposed control strategy will be presented in comparison with the conventional fixed dc voltage control.

4.1 Compensation results with adaptive dc voltage controlled APF

After compensated by the APF with adaptive dc voltage control strategy, the dynamic compensation process of the APF in both simulation and experiment are shown in Fig. 7, and the overall compensation results are listed in Tables 6 and 9. From Fig. 7, it can be observed that the dc-link voltage is adaptively controlled to different levels according to different loading conditions. The simulated and experimental PF,

THD_{isx} and i_{sn} can be improved to 0.98 or above, within 12% and significantly reduced after APF compensation for both loadings case, compared with Fig. 6. Moreover, the system current i_{sx} is significantly reduced after the APF compensation.

4.2 Comparison between fixed and adaptive dc-link voltage control

After compensated by the APF with fixed V_{dcU}, V_{dcL} =300V, the dynamic compensation process of the APF in both simulation and experiment are shown in Fig. 8, and the overall compensation results are listed in Tables 7 and 10. Compared Fig. 8 with Fig. 7 as well as Tables 7 and 10 with Tables 6 and 9, the fixed and adaptive dc voltage control can obtain almost the same steady-state compensation results. But the proposed control strategy solely requires lower dc voltage levels for compensating the 1st loading and the 1st together with the 2nd loadings as shown in Figs. 7 – 8. Thus, it obtains less THD_{isx}, i_{sn} and i_{sx} values for both loading cases, because a lower dc-link voltage will generate less switching noise into the system, and vice versa. For the proposed control strategy, due to its final reference V_{dc}^* is varying at different loading cases, the compensating performance is affected at each V_{dc} varying. Compared with the conventional one, the adaptive one obtains a longer settling time during both the loading and V_{dc} level varying case. Moreover, its dynamic response will be sacrificed a little bit under an adaptive low dc operating voltage.

Fig. 9 shows the APF experimental compensating current i_{cx} of phase a with: (a) fixed V_{dcU}, V_{dcL} =300V control and (b) adaptive dc voltage control during the 1st loading connected case, (c) fixed V_{dcU}, V_{dcL} =300V control and (d) adaptive dc voltage control during the 1st together with the 2nd loadings connected case. Fig. 9 shows that the proposed adaptive control strategy can effectively lower the switching noise of the APF in comparison to the conventional fixed V_{dcU}, V_{dcL} =300V operation. Moreover, from Table 11, the adaptive control strategy can reduce the inverter power loss by 37% and 39%, respectively compared with the conventional fixed V_{dcU}, V_{dcL} =300V control. From Table 11, this adaptive dc control technique should be more effective in APF application because it requires a high dc-link operating voltage compared with that of HAPF. Thus, the switching loss reduction for APF will be more significant.

From Figs. 6 – 9 and Tables 5–11, they verified that the proposed control strategy can significantly reduce the APF operational switching loss and switching noise and improve its compensation results without

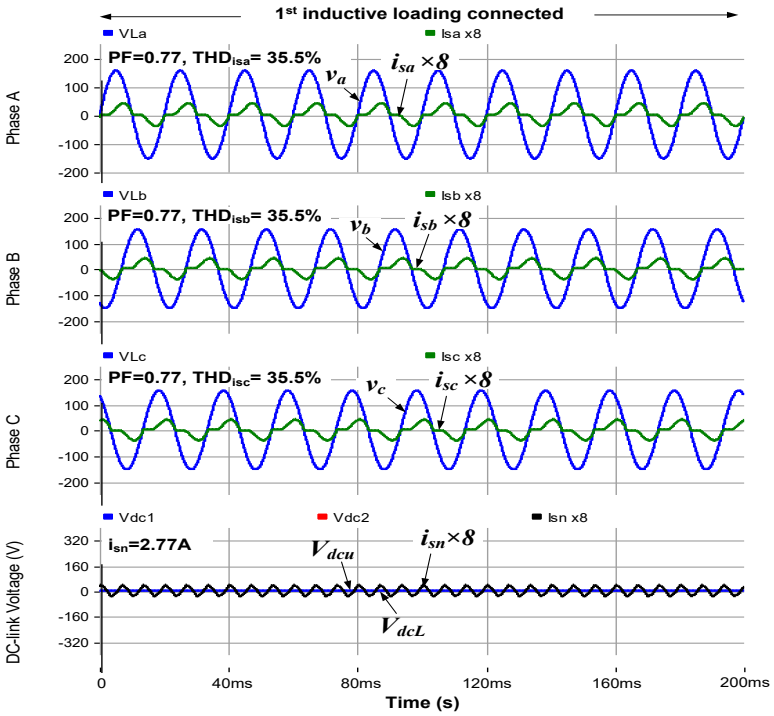
adding-in any soft-switching circuit.

The capacity of the testing APF system in this paper is small due to the laboratory facilities' limitations. As the reference compensating current in steady-state is the same for both conventional fixed and proposed adaptive dc-link voltage controlled APFs, the compensating current should be approximately the same. Thus, the inverter power loss reduction (efficiency enhancement) is mainly due to the dc-link voltage reduction. In addition, if the capacity (compensating current rating) of the APF system is larger, the trend of the power loss reduction still maintains because the difference between their inverter power losses is mainly due to the difference between their dc-link voltage levels.

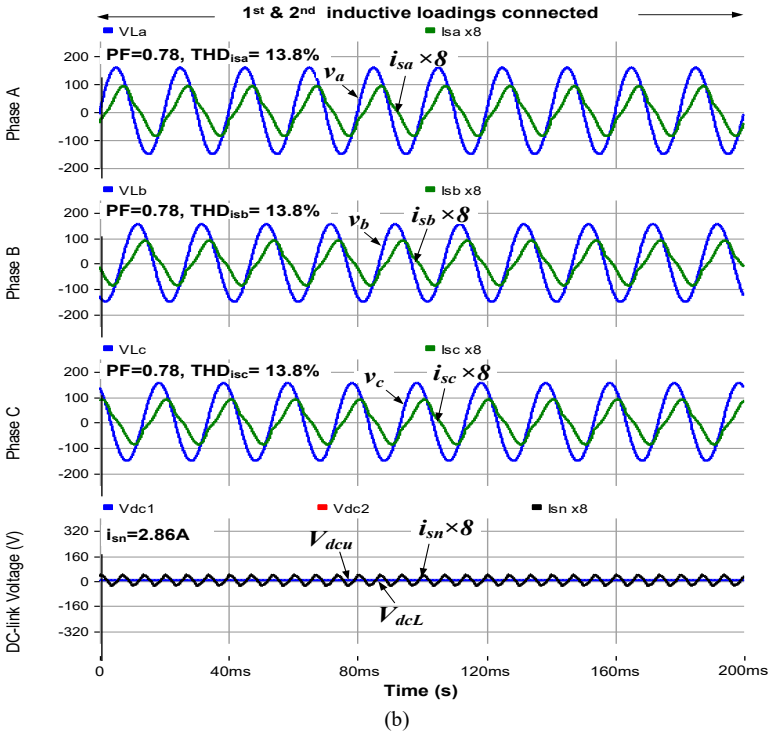
In addition, as this paper focuses on the APF application in low voltage power distribution side, the neutral wire presents, thus the proposed adaptive dc-link voltage control strategy for three-phase four-wire APF works even if the load is not connecting to the neutral point, such as: a three-phase AC to DC rectifier load or the load is in delta connection. Moreover, even though the change of the three phase loadings may not be identical, the proposed controlled APF can still compensate the reactive power and current harmonics problems. At the same time, the adaptive dc-link voltage control strategy can reduce the inverter part switching loss and switching noise in comparison with the conventional fixed dc-link voltage control.

5 Conclusion

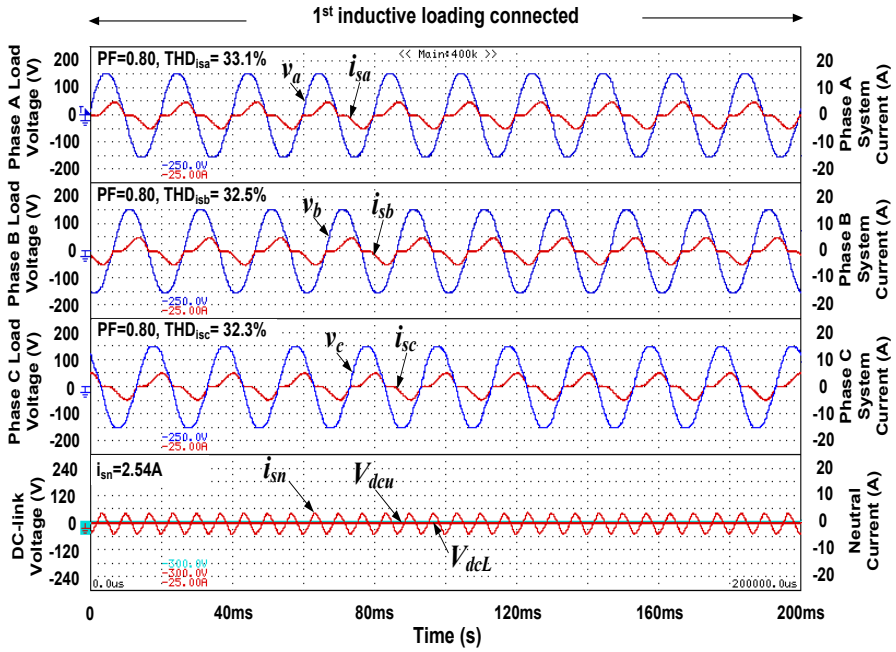
Soft-switching techniques are usually applied to reduce the operating switching loss of the high dc voltage controlled active power filter (APF). However, they all require extra auxiliary circuits, thus increasing the system initial cost. To obtain loss reduction function without adding extra circuit components, an adaptive dc voltage control strategy for active power filter (APF) is proposed. The dc voltage controller's design criteria including the stability study and dynamic performance analysis are discussed. In addition, the viability of the proposed controller for APF in lowering switching loss and switching noise is verified by both simulation and experimental results, compared with the traditional fixed dc voltage controlled APF and the APF with soft-switching auxiliary circuits.


1st inductive loading connected
VLa
Isa x8
PF=0.77, THDisa= 35.5%
va
isa ×8
Phase A
VLb
Isb x8
PF=0.77, THDisb= 35.5%
vb
isb ×8
Phase B
VLc
Isc x8
PF=0.77, THDisc= 35.5%
vc
isc ×8
Phase C
Vdc1
Vdc2
Isn x8
isn=2.77A
Vdcu
isn×8
VdcL
DC-link Voltage (V)
200
100
0
-100
-200
320
160
-160
-320
0
40ms
80ms
120ms
160ms
200ms
Time (s)

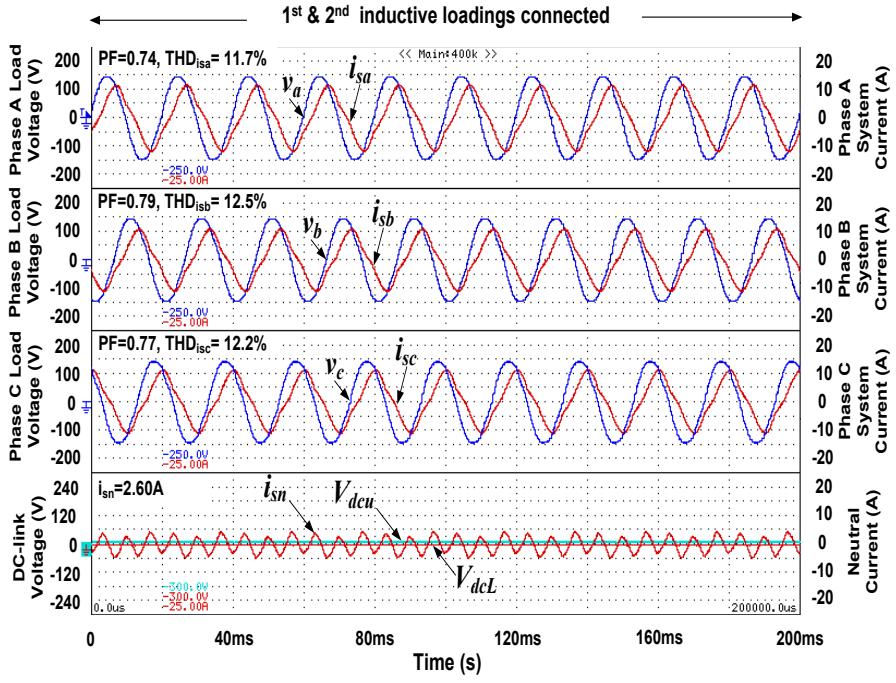
(a)


1st & 2nd inductive loadings connected
VLa
Isa x8
PF=0.78, THDisa= 13.8%
va
isa ×8
Phase A
VLb
Isb x8
PF=0.78, THDisb= 13.8%
vb
isb ×8
Phase B
VLc
Isc x8
PF=0.78, THDisc= 13.8%
vc
isc ×8
Phase C
Vdc1
Vdc2
Isn x8
isn=2.86A
Vdcu
isn×8
VdcL
DC-link Voltage (V)
200
100
0
-100
-200
320
160
-160
-320
0
40ms
80ms
120ms
160ms
200ms
Time (s)

(b)

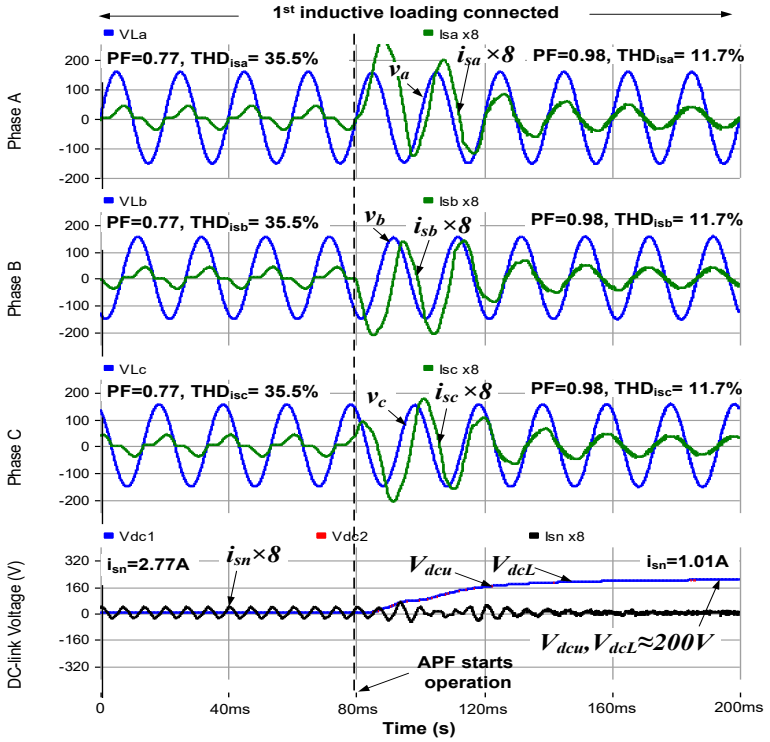


(c)

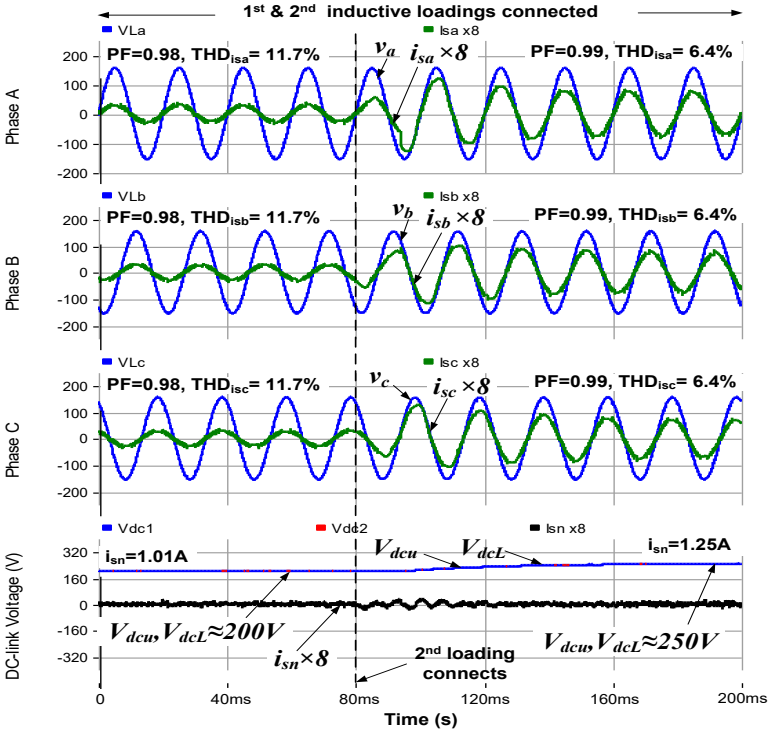


(d)

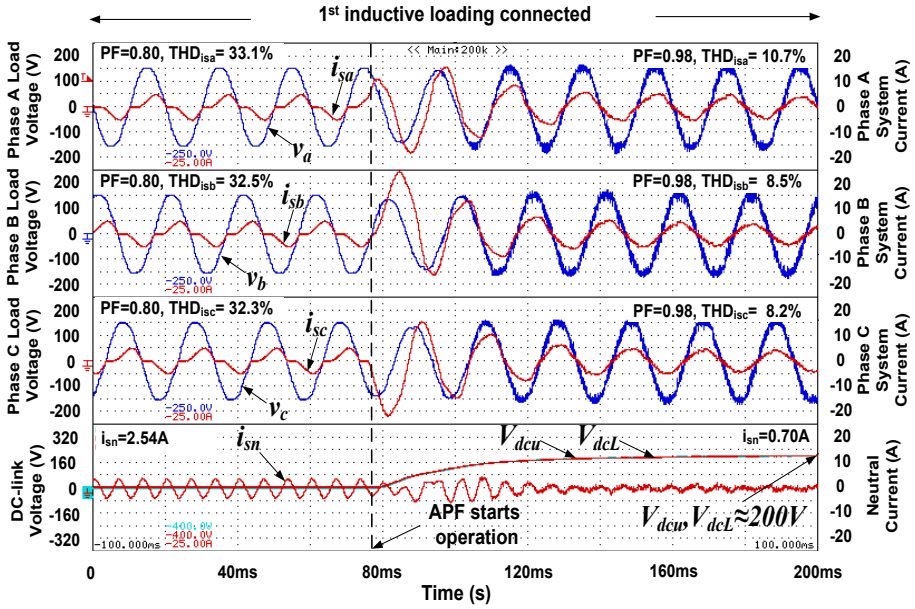
Fig. 6. Simulated and experimental PF, THD_{isx} and i_{sn} under different loading cases:
(a) Simulated PF, THD_{isx} and i_{sn} when 1st loading is connected,
(b) Simulated PF, THD_{isx} and i_{sn} when 1st and 2nd loadings are connected,
(c) Experimental PF, THD_{isx} and i_{sn} when 1st loading is connected,
(d) Experimental PF, THD_{isx} and i_{sn} when 1st and 2nd loadings are connected.


1st inductive loading connected
VLa
Isa x8
PF=0.77, THDisa= 35.5%
PF=0.98, THDisa= 11.7%
Phase A
VLb
Isb x8
PF=0.77, THDisb= 35.5%
PF=0.98, THDisb= 11.7%
Phase B
VLc
Isc x8
PF=0.77, THDisc= 35.5%
PF=0.98, THDisc= 11.7%
Phase C
Vdc1
Vdc2
Isn x8
isn=2.77A
isn=1.01A
Vdcu, VdcL≈200V
APF starts operation
DC-link Voltage (V)
Time (s)

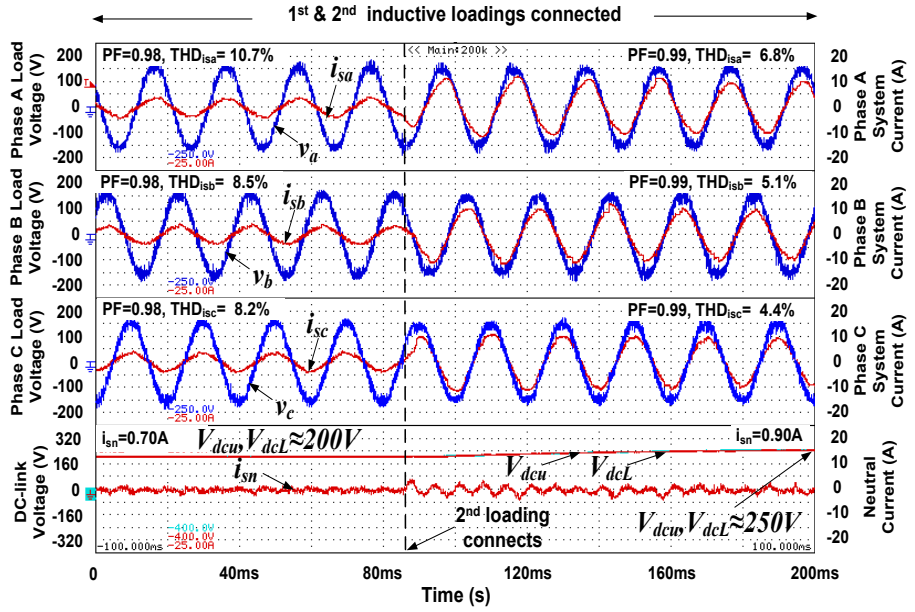
(a)


1st & 2nd inductive loadings connected
VLa
Isa x8
PF=0.98, THDisa= 11.7%
PF=0.99, THDisa= 6.4%
Phase A
VLb
Isb x8
PF=0.98, THDisb= 11.7%
PF=0.99, THDisb= 6.4%
Phase B
VLc
Isc x8
PF=0.98, THDisc= 11.7%
PF=0.99, THDisc= 6.4%
Phase C
Vdc1
Vdc2
Isn x8
isn=1.01A
isn=1.25A
Vdcu, VdcL≈200V
Vdcu, VdcL≈250V
2nd loading connects
DC-link Voltage (V)
Time (s)

(b)

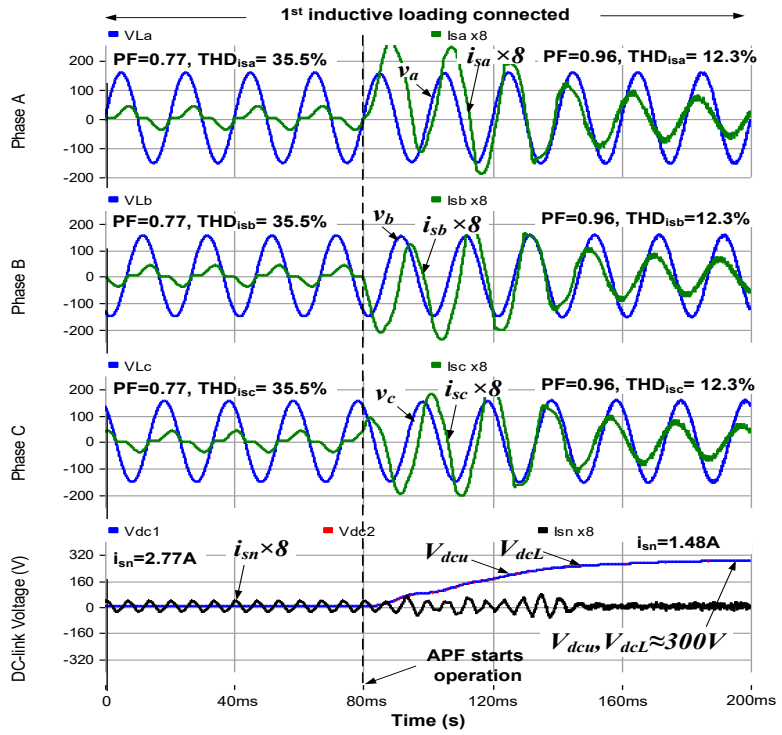


(c)

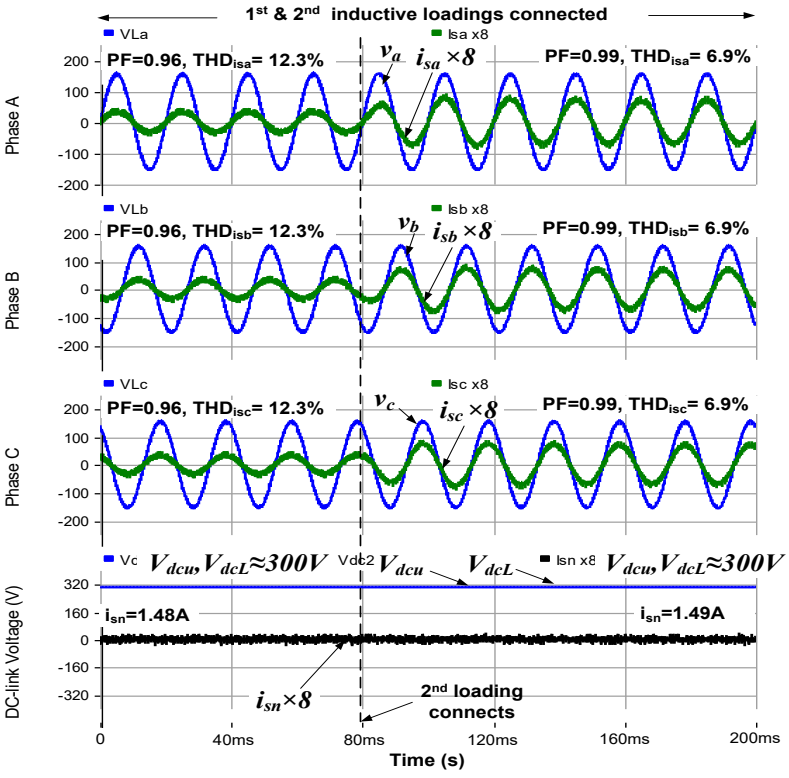


(d)

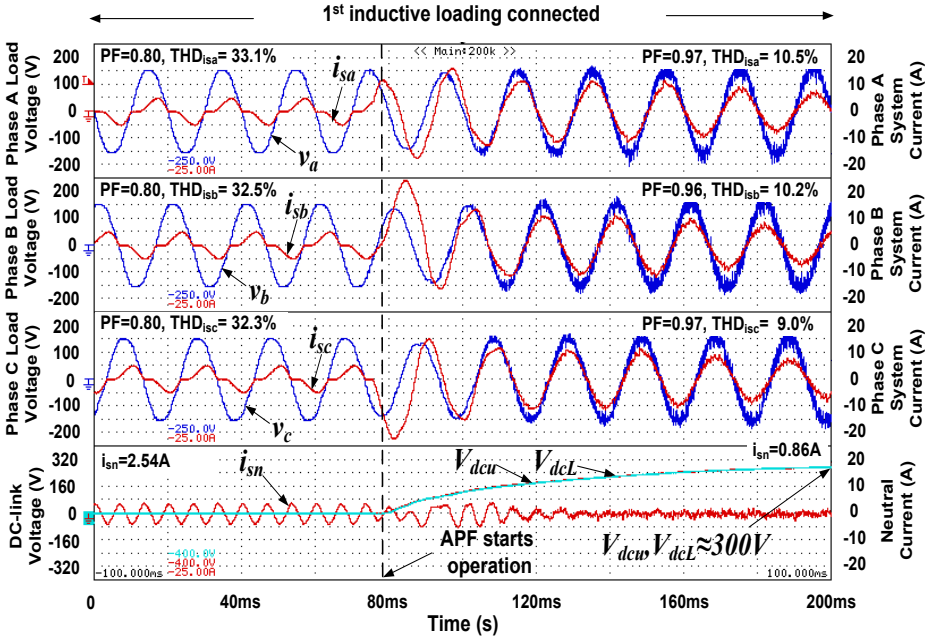
Fig. 7. Dynamic compensation process of the APF in both simulation and experiment with adaptive dc voltage control:
(a) Simulated PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} before and after APF starts operation during 1st loading,
(b) Simulated PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} when 2nd loading is connected,
(c) Experimental PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} before and after APF starts operation during 1st loading,
(d) Experimental PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} when 2nd loading is connected.


1st inductive loading connected
VLa
Isa x8
PF=0.77, THDisa= 35.5%
va
isa ×8
PF=0.96, THDisa= 12.3%
Phase A
VLb
Isb x8
PF=0.77, THDisb= 35.5%
vb
isb ×8
PF=0.96, THDisb=12.3%
Phase B
VLc
Isc x8
PF=0.77, THDisc= 35.5%
vc
isc ×8
PF=0.96, THDisc= 12.3%
Phase C
Vdc1
Vdc2
Isn x8
isn=2.77A
isn×8
Vdcu
VdcL
isn=1.48A
Vdcu,VdcL≈300V
APF starts operation
DC-link Voltage (V)
200
100
0
-100
-200
320
160
-160
-320
0
40ms
80ms
120ms
160ms
200ms
Time (s)

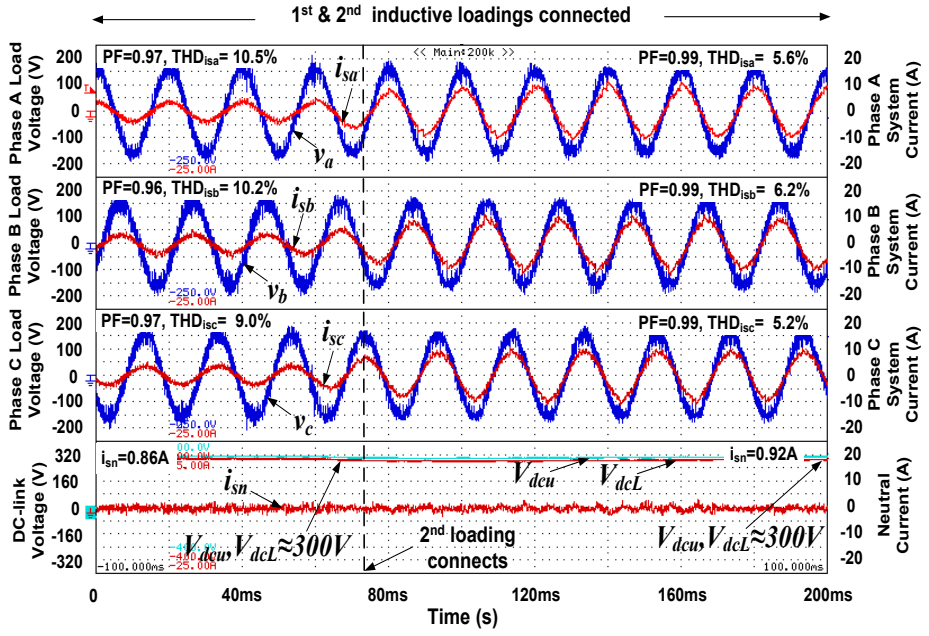
(a)


1st & 2nd inductive loadings connected
VLa
Isa x8
PF=0.96, THDisa= 12.3%
va
isa ×8
PF=0.99, THDisa= 6.9%
Phase A
VLb
Isb x8
PF=0.96, THDisb= 12.3%
vb
isb ×8
PF=0.99, THDisb= 6.9%
Phase B
VLc
Isc x8
PF=0.96, THDisc= 12.3%
vc
isc ×8
PF=0.99, THDisc= 6.9%
Phase C
Vc
Vdcu,VdcL≈300V
Vdc2
Vdcu
VdcL
Isn x8
Vdcu,VdcL≈300V
isn=1.48A
isn=1.49A
isn×8
2nd loading connects
DC-link Voltage (V)
200
100
0
-100
-200
320
160
-160
-320
0
40ms
80ms
120ms
160ms
200ms
Time (s)

(b)



(c)



(d)

Fig. 8. Dynamic compensation process of the APF in both simulation and experiment with fixed V_{dcU}, V_{dcL} = 300V:
(a) Simulated PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} before and after APF starts operation during 1st loading,
(b) Simulated PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} when 2nd loading is connected,
(c) Experimental PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} before and after APF starts operation during 1st loading,
(d) Experimental PF, THD_{isx}, i_{sn} and V_{dcU}, V_{dcL} when 2nd loading is connected.

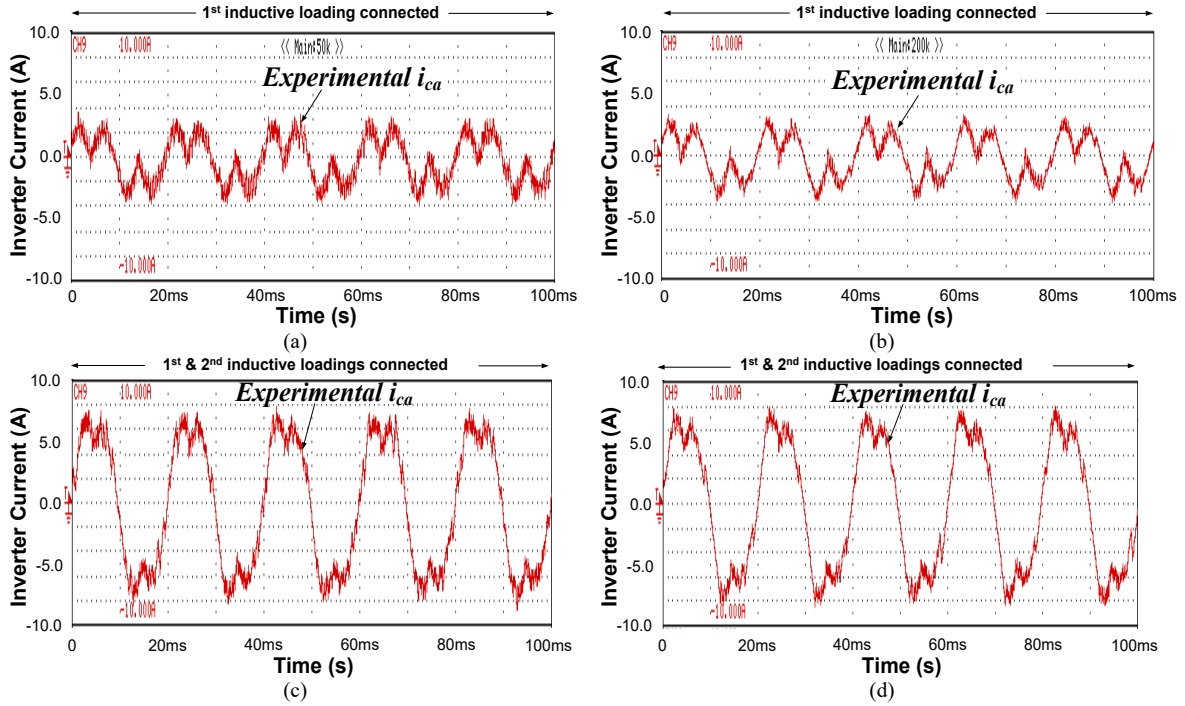


Fig. 9. Experimental i_{cx} of phase *a* with:
(a) fixed V_{dcU}, V_{dcL} = 300V control during 1st loading connected case,
(b) adaptive dc-link voltage control during 1st loading connected case,
(c) fixed V_{dcU}, V_{dcL} = 300V control during 1st and 2nd loadings connected case,
(d) adaptive dc-link voltage control during 1st and 2nd loadings connected case.

Table 5 Simulation results before APF compensation

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)
1st loading	A, B, C	175	0.77	0.82	35.5	2.94
1st and 2nd loadings	A, B, C	487	0.78	0.79	13.8	7.19

Table 6 Simulation results after APF compensation with adaptive dc voltage control strategy

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)	V_{dcU}, V_{dcL}
1st loading	A, B, C	-5	0.98	1.00	11.7	2.53	200V
1st and 2nd loadings	A, B, C	-4	0.99	1.00	6.4	5.94	250V

Table 7 Simulation results after APF compensation with conventional fixed dc voltage control strategy

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)	V_{dcU}, V_{dcL}
1st loading	A, B, C	-7	0.96	1.00	12.3	2.85	300V
1st and 2nd loadings	A, B, C	-2	0.99	1.00	6.9	6.11	300V

Table 8 Experimental results before APF compensation

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)
1st loading	A	191	0.80	0.85	33.1	2.83
	B	192	0.80	0.85	32.5	2.88
	C	187	0.80	0.85	32.3	2.84
1st and 2nd loadings	A	530	0.74	0.76	11.7	7.45
	B	450	0.79	0.80	12.5	7.02
	C	460	0.77	0.79	12.2	7.04

Table 9 Experimental results after APF compensation with adaptive dc voltage control strategy

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)	V_{dcU}, V_{dcL}
1st loading	A	51	0.98	1.00	10.7	2.46	200V
	B	52	0.98	1.00	8.5	2.39	
	C	48	0.98	1.00	8.2	2.45	
1st and 2nd loadings	A	80	0.99	1.00	6.8	6.01	250V
	B	100	0.99	1.00	5.1	5.90	
	C	80	0.99	1.00	4.4	6.02	

Table 10 Experimental results after APF compensation with conventional fixed dc voltage control strategy

Different cases		Q_{sxf} (var)	PF	DPF	THD_{isx} (%)	i_{sx} (A)	V_{dcU}, V_{dcL}
1st loading	A	70	0.97	1.00	10.5	2.53	300V
	B	78	0.96	1.00	10.2	2.57	
	C	71	0.97	1.00	9.0	2.57	
1st and 2nd loadings	A	100	0.99	1.00	5.6	6.11	300V
	B	120	0.99	1.00	6.2	6.17	
	C	110	0.99	1.00	5.2	6.17	

Table 11 Experimental inverter power loss of APF with fixed V_{dcu}, V_{dcL} =300V and adaptive dc voltage control

Inverter power loss of APF		Fixed V_{dcU}, V_{dcL} = 300V	Adaptive dc
Power loss (W)	1st loading	186.6W	118.2W (200V) ~37%↓
	1st and 2nd loadings	368.4W	223.2W (250V) ~39%↓

References

[1] Q.-N. Trinh, H.-H. Lee, "An advanced current control strategy for three-phase shunt active power filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5400 – 5410, Dec. 2013.

[2] S. T. Senini, and P. J. Wolfs, "Systematic identification and review of hybrid active filter topologies," in *Proc. IEEE 33rd Annual Power Electronics Specialists Conf., PESC. 02*, vol. 1, 2002, pp. 394–399.

[3] S. Rahmani, N. Mendalek, K. Al-Haddad, "Experimental design of a nonlinear control technique for three-phase shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3364 – 3375, Oct. 2013.

[4] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, P. Garcia-Gonzalez, "Application of a repetitive controller for a three-phase active power filter," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 237 – 246, Jan. 2007.

[5] S.K. Chauhan, M.C. Shah, R.R. Tiwari, P.N. Tekwani, "Analysis, design and digital implementation of a shunt active power filter with different schemes of reference current generation," *IET Power Electron.*, vol. 7, no. 3, pp. 627–639, Mar. 2014.

[6] Y. Suresh, A.K. Panda, M. Suresh, "Real-time implementation of adaptive fuzzy hysteresis-band current control technique for shunt active power filter," *IET Power Electron.*, vol. 5, no. 7, pp. 1188–1195, Aug. 2012.

[7] Zhenfeng Xiao, Xiangtian Deng, Rongxiang Yuan, Pilong Guo, Qijuan Chen, "Shunt active power filter with enhanced dynamic performance using novel control strategy," *IET Power Electron.*, vol. 7, no. 12, pp. 3169–3181, Dec. 2014.

[8] L.B. Garcia Campanhol, S.A. Oliveira da Silva, A. Goedtel, "Application of shunt active power filter for harmonic reduction and reactive power compensation in three-phase four-wire systems," *IET Power Electron.*, vol. 7, no. 11, pp. 2825–2836, Nov. 2014.

[9] S. Gomez Jorge, C.A. Busada, J. Solsona, "Reduced order generalised integrator-based current controller applied to shunt active power filters," *IET Power Electron.*, vol. 7, no. 5, pp. 1083–1091, May 2014.

[10] P. Kanjiya, V. Khadkikar, H.H. Zeineldin, "A noniterative optimized algorithm for shunt active power filter under distorted and unbalanced supply voltages," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5376 – 5390, Dec. 2013.
[11] R.L. de Araujo Ribeiro, C.C. de Azevedo, R.M. de Sousa, "A robust adaptive control strategy of active power filters for power-factor correction, harmonic compensation, and balancing of nonlinear loads," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 718 – 730, Feb. 2012.
[12] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 6, pp. 1312 – 1322, Nov./Dec., 1996.
[13] H. Akagi, "Modern active filters and traditional passive filters," *Bulletin of the Polish Academy of Sciences*, *Technical Sciences*, vol. 54, no. 3, pp. 255 – 269, 2006.
[14] L. Asiminoaei, P. Rodriguez, F. Blaabjerg, M. Malinowski, "Reduction of switching losses in active power filters with a new generalized discontinuous-PWM strategy," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 467 – 471, Jan. 2008.
[15] Specification of Honeywell SmartWave APF: http://www.honeywell-powercontrol.com/English/ Product_APF.aspx#
[16] Specification of ABB Power Quality Filters PQFI-PQFM-PQFS: http://www.abb.com/product/seitp329/ e83ed739e0daa5a9c1256f85004e548b.aspx?productLanguage=us&country=00
[17] Specification of INJET APF: http://www.injet.cn/en/content/ ?338.html
[18] Jie Chang, Jun Hu, "Modular design of soft-switching circuits for two-level and three-level inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp.131–139, Jan. 2006.
[19] D.M. Divan, G. Venkataramanan, R.W.A.A. DeDoncker, "Design methodologies for soft switched inverters," *IEEE Trans. Ind. Applicat.*, vol. 29, no. 1, pp. 126 – 135, Jan. 1993.
[20] R.W. De Doncker, J.P. Lyons, "The auxiliary resonant commutated pole converter," *Conf. Record of IEEE Industry Applicat. Society Annual Meeting*, vol. 2, Oct. 1990, pp. 1228 – 1235.
[21] L. Asiminoaei, F. Blaabjerg, S. Hansen, P. Thogersen, "Adaptive compensation of reactive power with shunt active power filters," *IEEE Trans. Ind. Applicat.,* vol. 44, no. 3, pp. 867-877, May/Jun., 2008.
[22] M.-C. Wong, J. Tang, Y.-D. Han, "Cylindrical coordinate control of three-dimensional PWM technique in three-phase four-wired trilevel inverter," *IEEE Trans. Power Electron.*, vol. 18, pp. 208 – 220, Jan. 2003.
[23] K.-W. Lao, N.-Y. Dai, W.-G. Liu, M.-C. Wong, "Hybrid power quality compensator with minimum dc operation voltage design for high-speed traction power systems," *IEEE Trans. Power Electron.*, vol. 28, no, 4, pp. 2024 - 2036, Apr. 2013.
[24] C.-S. Lam, W.-H. Choi, M.-C. Wong, Y.-D. Han, "Adaptive dc-link voltage controlled hybrid active power filters for reactive power compensation," *IEEE Trans. Power Electron.*, vol. 27, no, 4, pp. 1758 – 1772, Apr. 2012.
[25] C.-S. Lam, X.-X. Cui, W.-H. Choi, M.-C. Wong, Y.-D. Han, "Minimum inverter capacity design for three-phase four-wire LC-hybrid active power filters", *IET Power Electron.*, vol. 5, no. 7, pp. 956 – 968, Aug. 2012.
[26] C.-S. Lam, M.-C. Wong, W.-H. Choi, X.-X. Cui, H.-M. Mei, J.-Z. Liu, "Design and performance of an adaptive low-dc-voltage-controlled LC-hybrid active power filter with a neutral inductor in three-phase four-wire power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no, 6, pp. 2635 – 2647, Jun. 2014.
[27] C.-S. Lam, X.-X. Cui, M.-C. Wong, Y.-D. Han, "Minimum DC-link voltage design of three-phase four-wire active power filters", *2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2012.
[28] H. Akagi, S. Ogasawara, Kim Hyosung, "The theory of instantaneous power in three-phase four-wire systems: a comprehensive approach," *in Conf. Rec. IEEE-34th IAS Annu. Meeting*, 1999, vol. 1, pp. 431–439.
[29] V. Khadkikar, A. Chandra, and B.N. Singh, "Generalized single-phase p-q theory for active power filtering: simulation and DSP-based experimental investigation," *IET Power Electron.*, vol. 2, no. 1, pp. 67–78, Jan. 2009.
[30] L. H. Wu, F. Zhuo, P. B. Zhang, H. Y. Li, Z. A. Wang, "Study on the influence of supply-voltage fluctuation on shunt active power filter," *IEEE Trans. Power Del.*, vol. 22, pp. 1743–1749, Jul. 2007.
[31] W.-H. Choi, C.-S. Lam, M.-C. Wong, Y.-D. Han, "Analysis of dc-link voltage controls in three-phase four-wire hybrid active power filters," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2180 – 2191, May 2013.
[32] C.-S. Lam, M.-C. Wong, Y.-D. Han, "Hysteresis current control of hybrid active power filters," *IET Power Electron.*, vol. 5, no. 7, pp. 1188–1195, Aug. 2012.
[33] M. Aredes, J. Hafner, K. Heumann, "Three-phase four-wire shunt active filter control strategies," *IEEE Trans. Power Electron.*, vol. 12, pp. 311 – 318, Mar. 1997.
[34] Studio of Electricians, *Electrician Common Data Handbook*, Shanghai Science and Technology Press, 2013, ISBN 9787547816646.

[35] Ning-Yi Dai, Man-Chung Wong, “Design considerations of coupling inductance for active power filters”, *The 6th IEEE Conference on Industrial Electronics and Applications (ICIEA2011)*, Beijing, China, Jun. 2011, pp. 1370 – 1375.
[36] C. Xiao, G. Chen, W. G. Odendaal, ‘Overview of power loss measurement techniques in power electronics systems,’ *IEEE Trans. Ind. Appl.,* vol. 43, no.3, pp. 657-664, 2007.