

High-speed distance relaying using least error squares method and testing with FPGA

ISSN 1751-8687

Received on 14th January 2019

Revised 14th April 2019

Accepted on 22nd May 2019

E-First on 23rd July 2019

doi: 10.1049/iet-gtd.2019.0088

www.ietdl.org

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Abstract: The demand for high-speed protective relaying in modern power grids is growing. A relay's fast and secure operation to clear faults is critical, especially for EHV/UHV transmission systems (400 kV and above). This research proposes a sub-cycle distance relaying, which is based on the least error squares (LES) method, and with a data interface module implemented on field programmable gate array (FPGA). Taking advantage of inherent parallelism and pipelined architecture of the FPGA, the proposed relay design can support real-time data communications. Also, the flexible and reliable feature of the LES algorithm allows the proposed relay to make a fast and secure trip decision in different scenarios. The case studies demonstrate the effectiveness of the LES-based relay.

1 Introduction

A protective relay is a vital device in electrical power systems to alert or isolate faults by detecting abnormal conditions and sending a trip command, which has to be quick and secure. The security requirement means the relay should be able to identify and respond to real faults, but should not respond to events such as sudden load changes or system transients during normal operation. Regarding speed, primary relaying systems typically operate in one to one-and-a-half cycles. Some of the latest research shows that a one-millisecond reduction in tripping time can increase the power transfer by 15 MW [1], which is equivalent to saving one new distribution feeder.

Fast algorithms for detecting a fault and identifying the type of fault has been one of the hottest topics for research in the power system protection area for the past several decades. Most of the protection principles are based on the estimation of fundamental frequency components (phasors) of voltages and currents. The classical full cycle discrete Fourier transform (FCDFT) algorithm cannot effectively remove the DC decaying component due to its non-periodic property. In [2], an improved FCDFT is proposed, and it takes one cycle plus two samples to obtain an accurate estimation of the fundamental when the DC component is present. Besides FCDFT, several other modified sub-cycle methods have been proposed in [3–10]. In [3], a half-cycle discrete Fourier transform (HCDFT) is developed where only samples from half-a-cycle are utilised to estimate the phasors; this significantly reduced the calculation time significantly compared to the classical type FCDFT. However, HCDFT loses the ability to reject even harmonics and remove the decaying DC component. In [4], three off-line look-up-tables are formed to estimate the decaying DC parameters. The look-up-table approach can find the time constant of the decaying DC component using anti-aliasing filters with a specific cut-off frequency. If the system parameters change, the decaying DC parameters would also change, and the filter parameters would have to be found again. Otherwise, some errors would be introduced in estimating the decaying DC parameters, which means errors in phasor estimation. In [5], a convolutional sparse autoencoder (CSAE) is used to learn features from voltage/current signals. Fault detection is done by applying a classifier on the feature vectors and the operation time is within one cycle. However, some of the system transients that could arise due to CT saturation and CCVT transient errors are not considered; these may affect the estimation accuracy and speed. Another linear estimation method found to be reliable in the literature is the Kalman filtering

technique [6]. The method is stable in the presence of noise and harmonics but takes almost one cycle to obtain a stable result. Also, a large number of computations are needed in each time step due to the use of a state transition matrix and a driving function matrix.

Wavelet transform (WT) techniques have also been introduced in digital distance protection. Using the WT multi-resolution analysis (MRA), [7], the fundamental frequency phasor can be extracted faster than an FCDFT. Even though the response is fast, the algorithm may become insecure as the impedance trajectories swing in and out of the protection zone before settling. To overcome this challenge, we need to reset the data window once a disturbance is detected, to deliver a more stable response. Moreover, a pre-band pass filter is added to remove the DC component, but a time delay is introduced.

The authors in [8, 9] describe a phaselet scheme and testing for transmission line distance protection. Phaselets are pieces of phasor obtained using partial integral with increasing data windows. They become more and more accurate when the window length becomes one full cycle. The focus of the phaselet method is to balance the speed and accuracy with a variable-length window. In [10], Jin *et al.* research a phaselet-based and an incremental-phasor methodology and tests with a real-time simulation tool RTDS.

Recently, transient components in time-domain have also been researched for high-speed relaying. The primary advantage of the transients-based relays is that they are less dependent on the source behaviour and are more dependent on the network they are protecting. This feature is potentially useful in applications with inverter-based sources, such as wind and solar, that do not have the same voltage and current behaviour as a conventional synchronous generator [11]. Two types of time-domain methods have appeared in the literature: incremental-quantity based, and travelling-wave based methods [1].

In terms of performance, for the incremental-quantity based method described in [12], the distance relaying function is consistently fast with the average operating time below 4 ms, while the directional relaying function operates consistently in about 2 ms. The limitation of this method is that it will not detect faults that create a small change in the fault point voltage, such as high-resistance faults. Also, the operating time may be slower than a quarter of a cycle for faults that occur close to the voltage zero crossing.

SchweitzerIII *et al.* [12] claim the operating times for the TW-based line protection elements are < 1 ms plus the channel time. However, these methods require high-fidelity voltages and currents

measurements or high-speed communications. In [13], the correlation coefficient of incremental voltage and current of fault-generated TWs within a specific window are used for directional protection, this method does not add any additional requirement to the network and the operating time is < 7 ms.

In this paper, the least error squares (LES) based distance relay scheme is developed to achieve a fast sub-cycle response. An effective data window length is found to obtain a quick and stable estimation of the phasor. The other innovative component of the research work is the hardware implementation of the proposed algorithm on FPGA. The parallel and pipelining features of FPGA are shown in the design diagram.

In Section 2, the LES-based distance relaying methodology is discussed. In Section 3, the hardware implementation of the proposed relay using FPGA is discussed. In Section 4, test results are given and followed by discussions. Conclusions are drawn in Section 5.

2 LES-based distance protective relay

To obtain the fundamental AC phasor and to remove the decaying DC component from fault current inputs, Sachdev and Baribeau [14] proposed an algorithm based on the LES for numerical relaying.

2.1 Principle of LES algorithm

The basic equations for parameter estimation can be represented as follows:

$$[A][x] - [m] = [e], \quad (1)$$

where A is an independent variable polynomial, x is the parameter to be estimated, m are the measurements and e is the error.

Thus, $[e]^T[e]$ is the sum of error squares. To make the sum minimum, its derivative is equated to zero. Therefore, we have

$$[x] = \left[[A]^T[A] \right]^{-1} [A]^T[m] = [A]_{\text{left}}^{-1}[m], \quad (2)$$

where $[A]_{\text{left}}^{-1}$ is the left inverse matrix of $[A]$.

Now let us analyse the output of a CT or current transformer during a fault. The waveform mostly consists of a fundamental frequency, harmonic components (second, third harmonic and some higher-order frequency), and a decaying DC component depending on the instant of the fault. An anti-aliasing or low-pass filters before the numerical relaying blocks the higher-order harmonics above the fifth harmonic frequencies.

To explain briefly the basic LES equations, a waveform to be analysed is expressed below as mostly consisting of fundamental frequency term and a decaying DC term

$$i = I_p \sin(\omega t + \theta) + I_0 e^{-t/\tau}, \quad (3)$$

It is reasonable to expand $e^{-t/\tau}$ by using a Taylor series and ignore the terms equal or higher than the second order considering t or sampling interval is small enough

$$i = I_p \sin(\omega t + \theta) + I_0 - I_0 \frac{t}{\tau}, \quad (4)$$

$$i = I_p \cos(\theta) \sin(\omega t) + I_p \sin(\theta) \cos(\omega t) + I_0 - I_0 \frac{t}{\tau}, \quad (5)$$

where I_p is the peak value of the fundamental frequency component, θ is the phase angle of the fundamental frequency component, I_0 is the magnitude of the DC offset at $t=0$, τ is the time constant of the decaying DC offset and ω is 2π times the frequency of the power system.

Since t is a constant and known in advance when the sampling rate is decided, it can be replaced by a series of $n\Delta t$, where Δt is the sampling interval. And i is the current measurement, which is also known. Now four parameters need to be estimated, which are I_p , θ , I_0 and τ . Comparing (2) and (4), we can develop the current phasor calculation equation as follows:

$$\begin{bmatrix} I_p \cos(\theta) \\ I_p \sin(\theta) \\ I_0 \\ -I_0 \Delta t / \tau \end{bmatrix} = \left[[A]^T[A] \right]^{-1} [A]^T[i], \quad (6)$$

where (see (7)). The number of rows from the matrix A is the same as the sampling window length of i . Since the number of unknowns is four, the minimum requirement for window length is four. With a varying data window, the speed and accuracy become a trade-off. Obviously, when the data window length is more, the accuracy would be more, i.e. the method will be able to attenuate noise or other higher harmonic components more effectively. However, it will take more time for the longer window method to detect a fault condition. On the other hand, when the window length is less than half a cycle, the fault detection would be faster, but the accuracy could also be compromised.

One major advantage of the least squares algorithm is the freedom of choosing a window size. In this research, the objective is to obtain a stable estimation of a phasor as soon as possible (less than one cycle). Considering the sampling rate is 64 samples/cycle or 3840 samples/s, so the window length is chosen to be 32, which is a half cycle. The effectiveness of half-cycle-window can be proven in the following section.

2.2 Relay architecture

The complete architecture of the LES-based distance relay is illustrated in Fig. 1. The general operation process is as follows: after obtaining the fault voltage and the current signal from off-line simulation data, the LES module estimates the fundamental magnitude and phase angle of the signals. The fault detection module uses the LES results of the current to detect the initiation of a fault, while the mho element module calculates the line impedance and makes a comparison with the reference impedance. If the calculated impedance value falls into the zone configuration, the trip delay routine feature is activated and monitors a couple of steady values to issue a final trip command, which makes the circuit breaker isolate the fault. In this section, each module is discussed, and its design details are presented in the following subsections.

2.3 LES module with DC offset removal

A three-phase power system can have ten distinct types of possible faults: a three-phase fault, three phase-to-phase faults, three phase-to-ground faults, and three double-phase-to-ground faults. To

$$[A] = \begin{bmatrix} \sin(-n\omega\Delta t) & \cos(-n\omega\Delta t) & 1 & -n \\ \sin(-(n-1)\omega\Delta t) & \cos(-(n-1)\omega\Delta t) & 1 & -(n-1) \\ \dots & \dots & \dots & \dots \\ \sin(0) & \cos(0) & 1 & 0 \\ \dots & \dots & \dots & \dots \\ \sin((n-1)\omega\Delta t) & \cos((n-1)\omega\Delta t) & 1 & (n-1) \\ \sin(n\omega\Delta t) & \cos(n\omega\Delta t) & 1 & n \end{bmatrix} \quad (7)$$

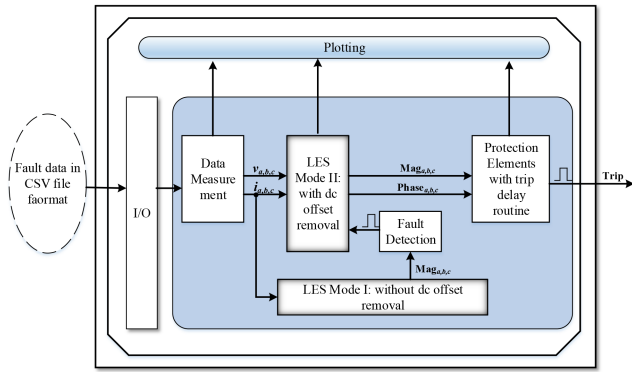


Fig. 1 Overall architecture to show (1) three main modules: fault detection, LES with/without dc offset removal, and protection elements with trip delay routine and (2) inputs/outputs

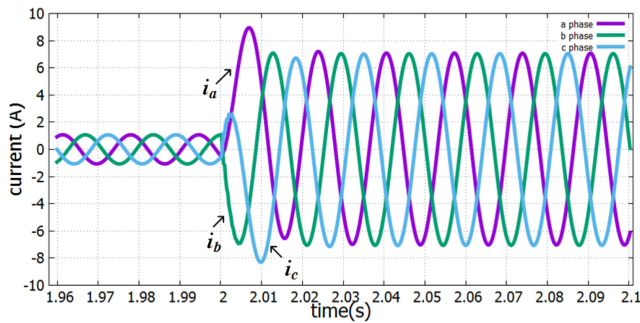


Fig. 2 Fault data generation

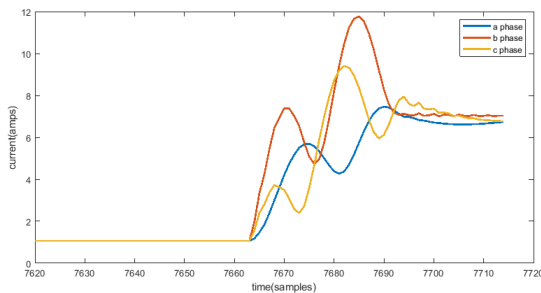


Fig. 3 LES current phasor for abc-to-ground fault

determine the fault type and make different trip decisions, we separately measured three-phase voltage and three-phase current. Generally speaking, two kinds of the sampling rate are used, a lower sampling rate of 64 samples/cycle and a higher sampling rate of 320 samples/cycle; these are respectively 3840 and 19,200 samples per second in a 60-Hz power system. Due to the high calculation complexity of the matrix-based LES algorithm, a lower sampling rate is utilised in this research. Fig. 2 shows the current measurement during the pre-fault and post-fault time range. Because it is a three-phase-to-ground fault, there are considerable magnitude surges on all of the three-phase currents. Implementing the calculation of fault impedance requires the fundamental frequency components of fault voltages and currents, and the moment of initiating the calculation depends on the fault detection results, which are based on the incremental changes of the current magnitude. Thus, LES estimation is a continuously running function and needs to operate in two modes: pre-fault and post-fault. In the pre-fault stage, LES estimation is utilised to obtain the current magnitude and the DC offset removal function is turned off, which can reduce the calculation burden and the resource requirement for implementing on FPGA hardware. After the fault detection (details will be presented in the next subsection about how the fault detection is done) signal is sent out, the LES estimation will be running for both current and voltage signals. In particular, DC offset removal is activated for fault current data. Fig. 3 shows the LES estimation procedure for a three-phase-to-

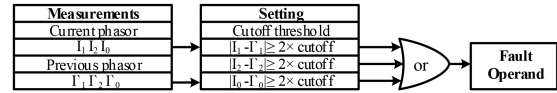


Fig. 4 Logic implementation of fault detection. $|I_1|'$, $|I_2|'$, and $|I_0|'$ are previous phasor magnitude from two cycles before

Table 1 Impedance equations based on different fault types

Relay elements	Impedance formula
$a - g$	$V_A / (I_A + 3m_0 I_0)$
$b - g$	$V_B / (I_B + 3m_0 I_0)$
$c - g$	$V_C / (I_C + 3m_0 I_0)$
$a - b$	$(V_A - V_B) / (I_A - I_B)$
$b - c$	$(V_B - V_C) / (I_B - I_C)$
$c - a$	$(V_C - V_A) / (I_C - I_A)$

ground fault. The system operates normally until a fault occurs at the 7664th sample, the LES estimation then converges at 7710th sample, so it takes 46 samples (0.72 cycles) to obtain a stable estimation.

2.4 Fault detection

In general, the parameters used to detect the initiation of faults include the magnitude of the current phasor, phase angles of the current and voltage, active and reactive power, the frequency of power system, and so on. In this case, the current magnitude is being monitored and tracked to detect the fault and trigger the protection process. This method is based on an over-current principle. The inputs of the fault detector are the present sequence currents and the corresponding measurements from two cycles earlier, as shown in Fig. 4. The magnitudes of the changes in these currents are evaluated against two times the cut-off threshold, which is set at 2% [15] of the steady-state value. If the change of any sequence current exceeds the limit, this demonstrates the transmission line is exposed to a disturbance situation and a fault detection signal is issued.

2.5 Protective elements

The relay in this research is designed to protect a transmission line with six impedance protection elements: three phase-to-ground elements and three phase-to-phase elements. Table 1 shows the apparent impedance calculation equations for different fault types. The factor m_0 is known as a compensation factor, which compensates the phase current for the mutual coupling between the faulted phase(s) and the other two(one) normal phases. All six of these elements are calculated after the fault detection signal is received. When a certain type of fault occurs, one or more of the elements are going to be activated to swing in an impedance diagram.

I_0 is zero sequence current calculated from $(I_A + I_B + I_C)/3$; $m_0 = (Z_0 - Z_1)/3Z_1$; Z_0 and Z_1 are zero and positive sequence line impedances from relay location to the protection zone, respectively.

2.6 Mho trajectory

The protective elements that would be activated for a fault can be analysed by looking at the impedance trajectory of the impedance value of the three-phases and the moment when it encroaches into the mho characteristic circle. A mho circle is selected because the transmission line is long and EHV type (reactance value is much greater than the resistance).

In general, there are three protection zones from zone 1 to zone 3 covering overlapped and extensive reach in one distance relay; moreover, they need to be set and coordinated operating together to make sure the transmission line is protected with back up. Because this research is focused on the high-speed feature of relays, only zone 1 is involved.

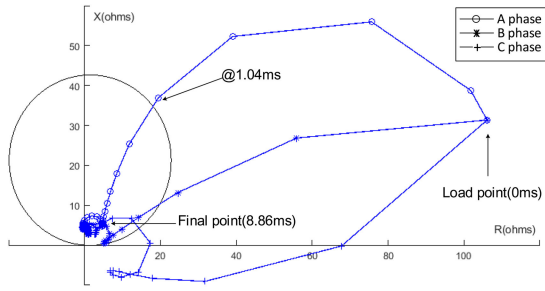


Fig. 5 Mho trajectory for phase abc-to-ground fault

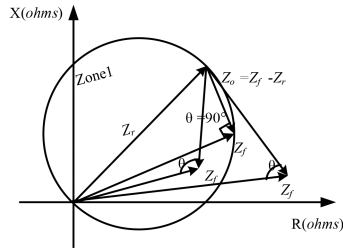


Fig. 6 Impedance comparison method

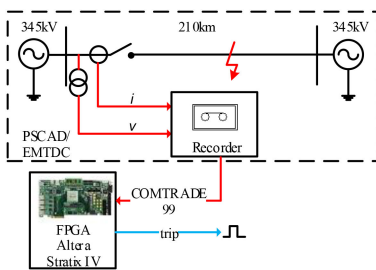


Fig. 7 Test platform for proposed relay

The impedance setting of the relay can be determined in this following principle; if Z_L is the positive impedance of the transmission line, and zone 1 protects 80% length of the line, n_i and n_e are the current transformer (CT) and voltage transformer (VT) turns ratios, then relay setting Z_r equals to $0.8 \times Z_L(n_i/n_e)$. The final mho characteristic is a circle passing through the origin and its diameter equals to $|Z_r|$.

After a fault occurs, the fault impedance Z_f will be calculated according to the LES estimation of voltage and current in every sampling step, so the Z_f is visualised as a trajectory moving in the impedance diagram ($R-X$ diagram). If the trajectory hits and settles into the mho characteristic circle, then it means that the fault happens in the zone 1 protection reach. For example, Fig. 5 shows the mho trajectory for a three-phase-to-ground fault. Noted that every time interval between two marks on the loci is a sampling step equals to 260 μ s.

2.6.1 Vector check: For the impedance comparison logic on a computer, the software calculates the angle between fault vector Z_f and operating vector $Z_o = Z_f - Z_r$. As can be seen from Fig. 6, if the angle is greater than or equal to 90° , the fault impedance Z_f is within or on the mho circle meaning the calculated impedance is under-reaching the zone. In this case, the relay will issue a trip decision (with a trip delay routine) to the circuit breaker to isolate the fault. For example, with two vectors ready, $Z_o = a + jb$ and $Z_f = c + jd$, the angle between them can be derived from $\cos \theta = ((Z_o \cdot Z_f) / (|Z_o| |Z_f|))$, where $Z_o \cdot Z_f$ is the inner product of two vectors in the Cartesian coordinate system. As the cosine value of 90° is zero, the sign of cosine value, determined by $Z_o \cdot Z_f$ the part which is $ac + bd$, can be an ideal indicator to determine whether the fault impedance is inside the mho circle zone.

2.6.2 Trip delay routine: This is another feature of mho trajectory module, and it is activated when the impedance trajectory enters into the mho circle at any time. It then waits for a subsequent few samples calculations and evaluates two conditions: (i) if the magnitude of change in impedance is small enough and (ii) the following consecutive impedances are also located inside the mho circle. If both of the conditions are met, a trip decision will be issued; otherwise, the trip delay routine would be reset to wait for the next activation.

3 Hardware implementation

In the last section, the distance relay is speeded up from a software perspective; for this section, the hardware-based techniques will be discussed.

In 2009, Zadeh *et al.* first developed distance relay on a field programmable analogue array (FPAA) platform [16]. Currently, a lot of research about field programmable gate array (FPGA) have been undertaken in the industrial control applications area [17], Valsan and Swarup [18] designed an FPGA-based transformer relaying, Liu *et al.* [19] proposed a protection scheme for HVDC line using FPGA, Wang and Dinavahi [20] implemented DFT-based protective relay on FPGA, Jin *et al.* [10] implemented phaselet-based protective relay on FPGA.

The test network is shown in Fig. 7. And the type of FPGA used for testing is Altera Stratix IV. The two major features for FPGA to improve speed and throughput are parallel processing and pipelining techniques. For parallel processing, FPGAs are simply arrays of programmable gates and so they can be combined into many individual hardware units with arbitrary size. Different operations can be processed at the same moment and do not need to compete for the same resources. For pipelining, operations can be inserted with Data Flip-flops (DFF) between steps to preserve the output of the last step for next step operation. Then, a critical path is assembled by wiring the inputs and outputs of each step into a line, so different steps in the critical path can operate at the same time.

These two features will be presented with a logic design case of a data interface module. There are two parts in this module: uploading fault signals in a COMTRADE 99 file from RAM to registers, and transforming the COMTRADE 99 format data into IEEE 754 standard floating-point binary data.

The goal of the logic design is to break down the functional module into combinational logic components or sequential logic flow. The combinational logic is made of several or/and/not digital logic gates and used for building a logical judgment branch, while sequential logic is used for general operation process, which is synchronised with clocks generated by crystal chips on FPGA. First, when a power system is simulated in PSCAD, there are two types of files generated simultaneously in COMTRADE 99 protocol: Setting file and Data file, which is shown in Fig. 8. When extracting fault data from the COMTRADE 99 files, the sample values y are calculated by using the equation $y = Mx + N$, where x is quantised records stored in Data files, which range from $-32,678$ to $32,677$, M and N are constants saved in Setting files. Next, to transform one certain x to y taking advantage of parallel processing, the calculation could be divided into three parallel paths: the sign and highest digit, two middle digits, and two lowest digits. Fig. 9 shows the design diagram. Then, for the longest time-consuming critical path, there are four steps of operations to be done sequentially: two adders and two multipliers. Since an adder costs two more clocks than a multiplier, a two-clock-delay DFF needs to be inserted between an adder and a multiplier to fulfil the pipelining feature. Therefore, in terms of one x , it takes 28 clock cycles to obtain the calculation result y . However, as the input x is given a new value, there will be a new result at every seven clock cycles until all the x in the COMTRADE file are transformed.

In terms of the latency, since the bandwidth of the interface for FPGA bus is 32-bit and the data are coded in 16-bit ASCII format, two digits of data can be transferred from RAM into registers every single clock. And the timing diagram (Fig. 10) shows that every 15 clocks, a sample value (-7310 in Fig. 8) is uploaded and transformed following such steps: (1) uploaded as three pairs of

digits; (2) broken down to higher and lower digit; (3) encoded and assembled to final output. Because there are six groups of data – three phases voltage and three phases current – need to be uploaded, then the total time of 90 clocks needs to be smaller than the sampling interval (260 μ s) to fulfil a real-time interface. On the other hand, the FPGA can work at 100 MHz clock rate (up to 156.25 MHz for this board [21]), so one clock takes 0.01 μ s. Because the uploading time for one sample of $90 \times 0.01 = 0.9 \mu$ s is much smaller than 260 μ s, the designed interface module can handle the data sampling in a real-time fashion.

4 Case study

To verify the effectiveness of the proposed distance relay design, we simulated several typical types of faults on two test power system, and used PSCAD/EMTDC® and RTDS® to generate the fault data, respectively. These off-line data are then fed into the target relay for testing and verification.

4.1 Two-bus system studies

The validated system consists of two synchronous generators and one transmission line, which is 210 km long. The system is shown in Fig. 11 with the parameters given below.

$V_{base} = 345 \text{ kV}$, $S_{base} = 100 \text{ MVA}$, fault impedance = 0.001 Ω ,
 Source parameters: $Z_s = 9 + j37.7 \Omega$, $E_{s1} = 345 \angle 0^\circ$,
 $E_{s2} = 345 \angle 30^\circ$,

Transmission line length: 210 km,
 Transmission line sequence impedance (Ω/km):
 $Z_0 = 0.363 + j1.323$, $Z_1 = 0.0358 + j0.5078$,
 $Z_2 = 0.0358 + j0.5078$,

Relay setting: $Z_r = 3.004 + j42.7 \Omega$. The proposed distance relay is tested for three scenarios of different fault locations, and each scenario consists of four fault types. Fig. 11 shows the configurations of three locations, which are Scenario 1-close to the relay, Scenario 2-barely within and Scenario 3-beyond the relay zone setting reach. For example, the first test case is a single-

- 1, 0, -7315
- 2, 260, -7314
- 3, 520, -7310
- 4, 780, -7303
- 5, 1040, -7312
- 6, 1300, -7323
- 7, 1560, -7337
- 8, 1820, -7347
- 9, 2080, -7352
- 10, 2340, -7359

Fig. 8 Fault data in COMTRADE 99 file

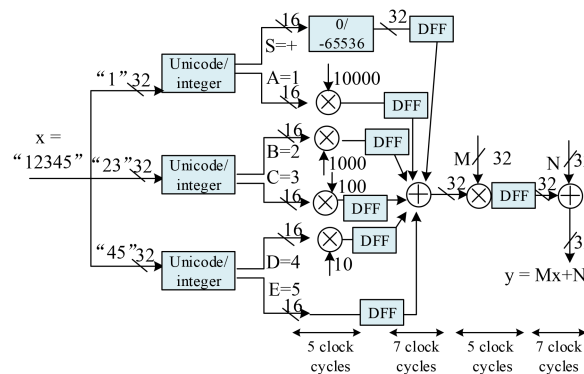


Fig. 9 Logic design diagram for data transformation

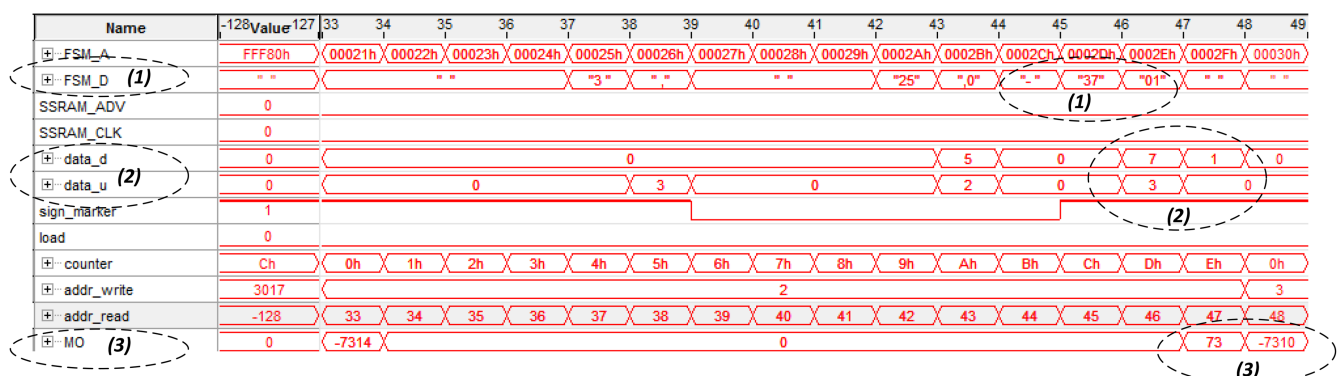


Fig. 10 Transformed data of single-floating format displayed in Quartus SignalTap simulation tool

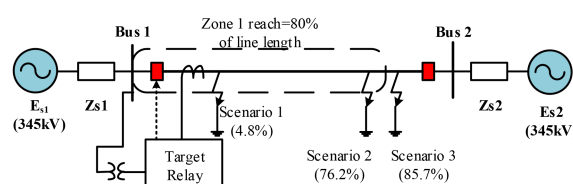


Fig. 11 Test project of transmission line in PSCAD

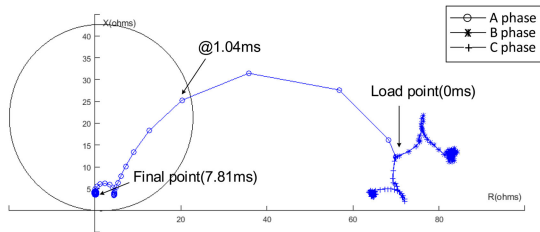


Fig. 12 Impedance trajectory of a-to-ground fault

Table 2 Tripping time of Scenario 1

Fault type	Tripping issued at	Time, ms	Time in cycles
three phase-g	34	8.86	0.53
a-ground	30	7.81	0.49
bc-ground	33	8.60	0.52
b-c	33	8.60	0.52

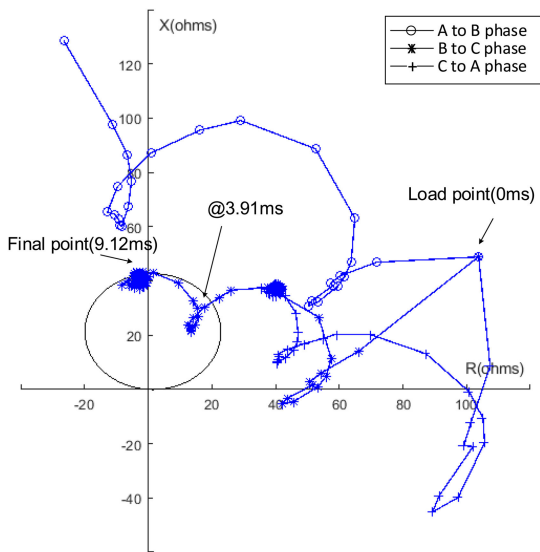


Fig. 13 Impedance trajectory of b-to-c fault

phase-to-ground fault which occurs at 10 km away from the relay location.

(i) *Scenario 1* (a fault occurs at 10 km, which is 4.8% of the transmission line): As shown in Fig. 12, before the fault occurs, the steady-state impedance $-66.7 + j12.8 \Omega$ is outside the mho characteristic circle. After a phase-a-to-ground fault is initiated, the phase-a impedance trajectory enters into the circle and converges to its final new steady state of $-1.2 + j4.8 \Omega$. When the trip delay routine check succeeds, which means the magnitude change of impedance is less than 1% and the operating point is staying within the zone circle for five samples, then the relay will issue a final trip signal at 30th sample, or tripping duration equals to 7.81 ms. Furthermore, for the phase-a-to-ground fault, only the impedance of phase-a moves into the circle, while the other two phase impedance loci stay at the original area during the pre-fault and post-fault period. A similar situation also fits the three-phase-to-ground fault and two-phase-to-ground fault. For the phase-to-phase fault, the impedance calculated should be phase-to-phase instead of the phase-to-ground element. The tripping time of the four types of faults is shown in Table 2, and all of them meet the sub-cycle requirement.

(ii) *Scenario 2* (a fault occurs at 160 km, which is 76.2% of the transmission line): The impedance trajectory for a b-to-c fault is shown in Fig. 13. In this case, since the fault occurs near the relay reach of the transmission line, the impedance trajectory enters the circle but keeps close to the edge of the circle. The tripping time of the four types is shown in Table 3, which are longer than in Scenario 1, but meet the sub-cycle requirement.

Table 3 Tripping time of Scenario 2

Fault Type	Tripping issued at	Time, ms	Time in cycles
three phase-g	48	12.50	0.75
a-ground	49	12.76	0.77
bc-ground	39	10.16	0.61
b-c	39	10.16	0.61

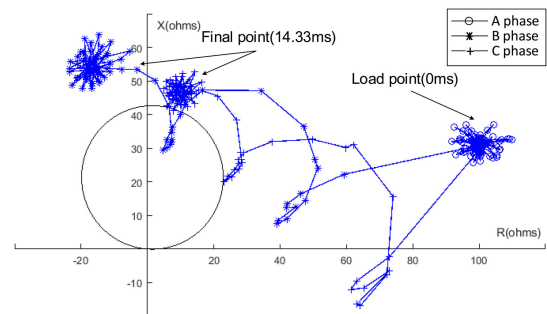


Fig. 14 Impedance trajectory of bc-to-ground fault

Table 4 Operating time improvement

Fault type	Proposed LES, ms	FC-DFT [19], ms	Orthogonal filter [22], ms	HC-DFT [23], ms
three phase-abc-g	12.50	22.14	17.50	14.17
a-g	12.76	25.12	17.50	14.17
b-c	10.16	22.89	16.84	13.17

(iii) *Scenario 3* (a fault occurs at 180 km, which is 85.7% of the transmission line): The impedance trajectory for a bc-to-ground fault is shown in Fig. 14. In this case, since the fault occurs out of the relay reach of the transmission line, the impedance trajectory does not enter the circle, which means the relay does not trip in this scenario.

The case studies discussed above show that the LES-based relay has the following features in terms of its performance and reliability:

(i) *Performance*: The most important finding is that, for different fault types and fault locations, the LES method operates within one cycle. For Scenario 1 where fault location is at the near end of the relay reach setting, the trip signals are sent out the fastest, at around 0.49–0.53 cycles. For Scenario 2, where fault location is on the far end of the relay reach setting, the trip signals are sent out at 0.61–0.77 cycles. These results are close to the operating time 0.6 cycles presented in [4], which also uses a LES method and the same sampling rate. Also, take Scenario 2 for example, the proposed LES method is compared with other methods and equipment such as FC-DFT [20], time-domain short-window orthogonal filters relay [22] and HC-DFT based relay [23]. Table 4 shows that the proposed LES method is considerably faster.

(ii) *Reliability*: LES technology correctly responds to different fault types and fault locations. When a specific kind of fault occurs, the corresponding impedance element(s) enter and settle in the mho circle, while the other impedance element(s) stay out of the mho circle. Furthermore, the impedance loci move into the circle when faults occur within the relay reach setting, while the impedance loci stay out of the circle when faults are initiated beyond the relay reach setting.

4.1.1 CT saturation: Abnormally high primary fault currents, primary fault currents with a DC offset, residual flux, high secondary burden (CT secondary load), or a combination of these factors results in the creation of high flux density in the CT magnetic core. When the density reaches or exceeds the design limits of the core, saturation occurs. At this point, the accuracy of

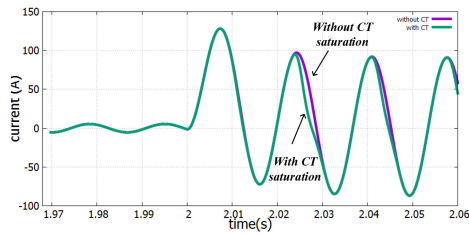


Fig. 15 Current with and without saturation

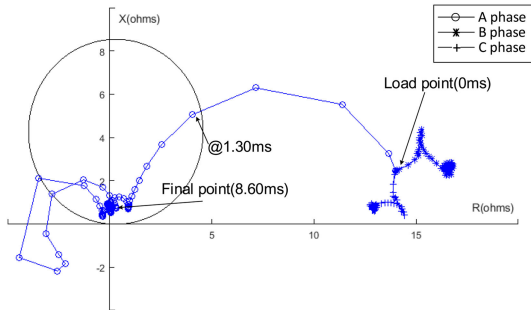


Fig. 16 Mho trajectory of a-ground fault under CT saturation

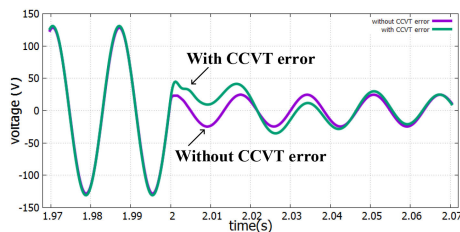


Fig. 17 Secondary voltage for zero-point-fault

the CT becomes poor, and the output waveform may be distorted. Saturation results in the production of a secondary current that is lower in magnitude than could be indicated by the CT ratio.

Consider a case with the CT ratio equal to 800:5, and a phase-a-to-ground fault happens at 10% of the relay reach setting. In this case, CT saturation has an observable impact compared to primary end faults. Fig. 15 shows that CT saturation barely introduces any waveform distortion with the first one-and-a-quarter cycle after fault initiation. After that period, the distortion is noticeable. Fig. 16 shows that impedance trajectory of the scenario. Then, we can see that the phase-a trajectory settles within the mho circle at 8.60 ms, just like it does in Scenario 1. However, after one-and-a-half cycles, it will start to swing out of the circle, and it takes five samples for it to swing into the circle again and settle around the original spot. In summary, because CT saturation does not occur instantly, the LES-based relay can operate quickly enough before severe distortion occurs.

4.1.2 CCVT transient: One of the most common voltage measurements for relaying, particularly at higher voltages, is the CCVT, coupling capacitor voltage transformer. A capacitor stack is used as a potential divider between the high-voltage apparatus and ground. Due to the tuned circuit used for compensation of the phase shift between the primary and secondary voltages, the secondary voltages may be significantly different from the primary voltages during transient conditions. Furthermore, CCVT output under faulted conditions become lower, so even a small transient component may cause problems for relaying applications. Fig. 17 shows that a single-line-to-ground fault is applied when instantaneous current is at the zero point; the transient waveforms are distorted just after the moment fault occurs. Whereas Fig. 18 shows that the fault is applied when instantaneous current is at the peak point. These two scenarios are the boundaries for all the possible fault angle situations.

In practice, the source impedance ratio (SIR) is a key factor causing the voltage to collapse when faults occur. IEEE C37.113,

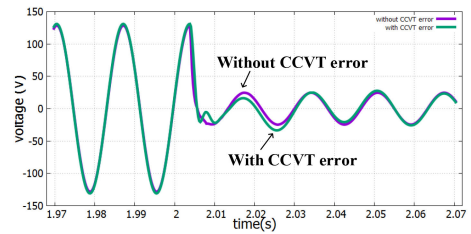


Fig. 18 Secondary voltage for peak-point-fault

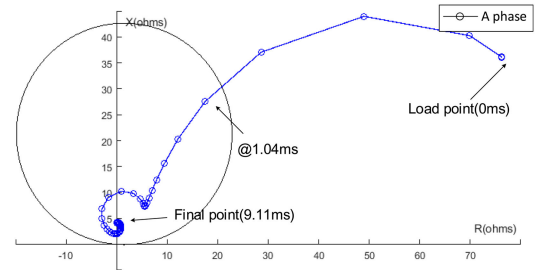


Fig. 19 Mho trajectory of zero-point fault in the transmission line which SIR = 4, no CCVT

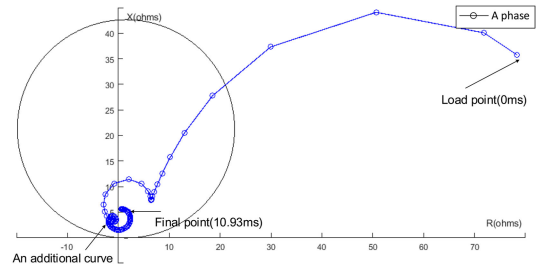


Fig. 20 Mho trajectory of zero-point fault in the transmission line which SIR = 4, with CCVT

IEEE Guide for Protective Relay Applications to Transmission Lines [24] classifies line length based on SIR as follows:

- Long line (SIR < 0.5).
- Medium line (0.5 < SIR < 4).
- Short line (SIR > 4).

In this case study, two scenarios where SIR = 4 and 10 are selected to analyse the relationship between SIR and relaying performance.

(i) *Scenario 1* (SIR = 4, fault angle = 0°): Figs. 19 and 20 show the impedance trajectories in this scenario. Comparing these two loci, it takes more 1.82 ms for the loci with CCVT to settle into stable value.

(ii) *Scenario 2* (SIR = 10, fault angle = 0°): Figs. 21 and 22 show the impedance trajectories in this scenario. If CCVT is a presence, the impedance locus swings out of the mho circle at 9.17 ms, and settles into the mho circle again at 19.50 ms with a slow convergence speed, which makes the trip signal to happen 0.65 cycles later compared to the 8.60 ms when the CCVT is not presence. Considering the SIR equaling to 10 is a quite extreme condition, a 0.7 cycles trip delay margin is needed to obtain the secure trip command. On the other hand, for the peak-point fault, the CCVT transient error does not have a noticeable impact on the tripping process.

4.2 IEEE 12-bus system – EHV composite model of Midwest Reliability Organization (MRO)

A larger 12-bus test power system from the MRO, shown in Fig. 23 is also used for verifying the performance of the LES method. This system configuration represents a composite model of Manitoba Hydro, North Dakota, Minnesota, and Chicago area subsystems. The line between Bus 7 and Bus 8 consists of two

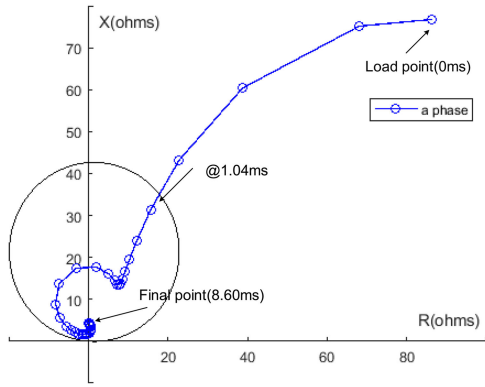


Fig. 21 Mho trajectory of zero-point fault in the transmission line which $SIR = 10$, no CCVT

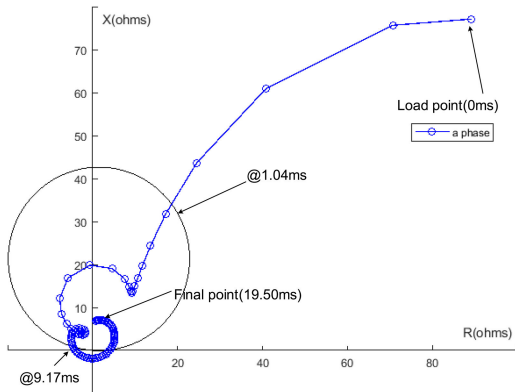


Fig. 22 Mho trajectory of zero-point fault in the transmission line which $SIR = 10$, with CCVT

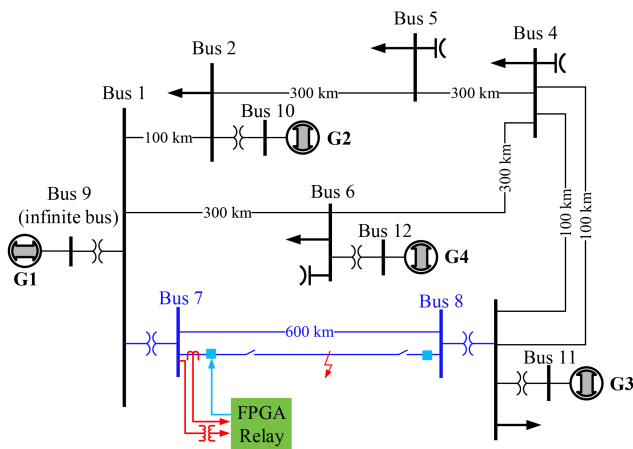


Fig. 23 IEEE-12 bus system used for testing

parallel 400 kV transmission lines. Jin *et al.* [10] give the line parameters, CT and CCVT modelling parameters in detail and are not being repeated here for brevity purposes.

Transmission line sequence impedance (Ω/km):
 $Z_0 = 0.208 + j0.6664$, $Z_1 = 0.0209 + j0.1813$,
 $Z_2 = 0.0209 + j0.1813$,

Relay setting: $Z_r = 0.39 + j3.35 \Omega$.

(i) *Scenario 1*: Fault occurs at 384 km, which is 64% of transmission line: The impedance trajectories for a-to-g and abc-to-g fault are shown in Figs. 24 and 25, and the corresponding trip times are 10.84 ms (0.65 cycles) and 13.54 ms (0.81 cycles).

(ii) *Scenario 2*: Fault occurs at 480 km, which is 80% of transmission line: The impedance trajectories for a-to-g and abc-to-g fault for this scenario are shown in Figs. 26 and 27. In this case, since the fault has occurred at the boundary of the relay reach, the impedance trajectory moves in and out of the circle. As a result, the

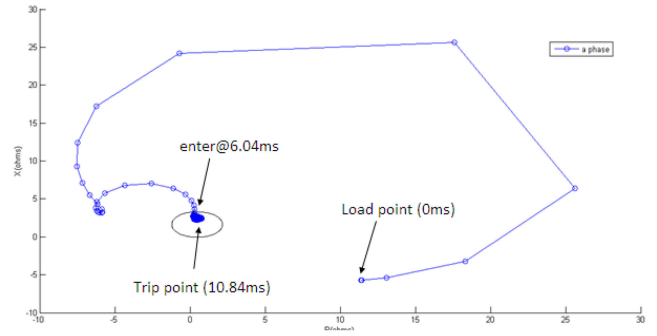


Fig. 24 Impedance trajectory for a-to-g fault at 384 km (64% of the transmission line)

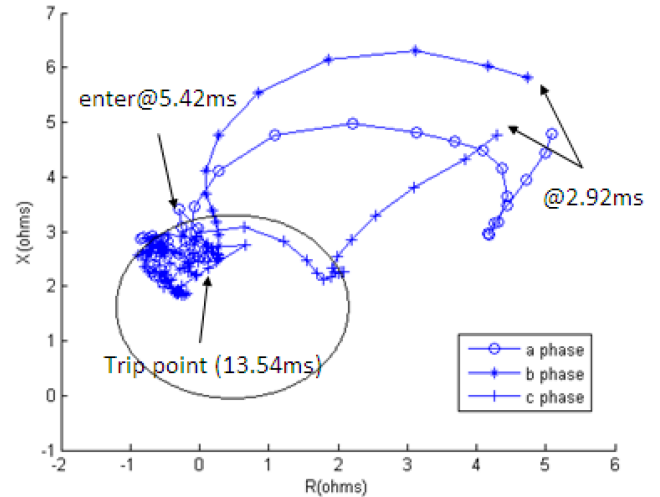


Fig. 25 Impedance trajectory of abc-to-g fault at 384 km (64% of the transmission line)

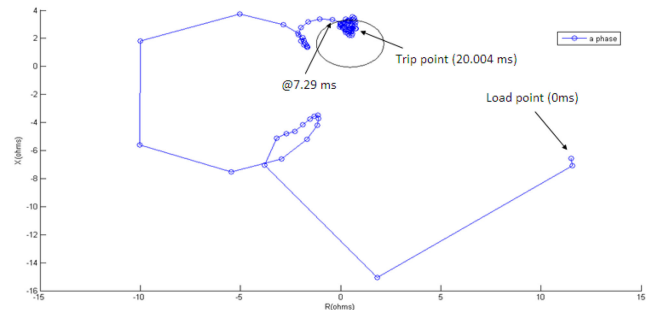


Fig. 26 Impedance trajectory of a-to-g fault at 480 km (80% of the transmission line)

trip decision could take much longer – 20.004 ms (1.2 cycles) and 14.79 ms (0.887 cycles), respectively, for the two cases. The faults on the relay boundary could take much longer to detect (which is one limitation of the phasor estimation algorithms).

4.2.1 Comparative analysis: LES method versus HCDFT method: Fig. 28 shows a comparative analysis of the LES performance versus the HCDFT method [3] for an a-g fault at 384 km. Firstly, from the figure, it can be seen that the trajectory of LES and HCDFT are different. They approach the final fault impedance point from different directions. This is due to the different formulations for the equations to estimate the voltage and current phasors with the two methods. Secondly, the tripping speeds are quite close, which is expected since both methods use the same sized filtering windows (half cycle). Finally, both methods approach the actual fault point ($0.2826 + j2.3602$), which verifies the results obtained using both methods.

Both methods use the same trip delay routine: 4.8 ms for the comparative studies.

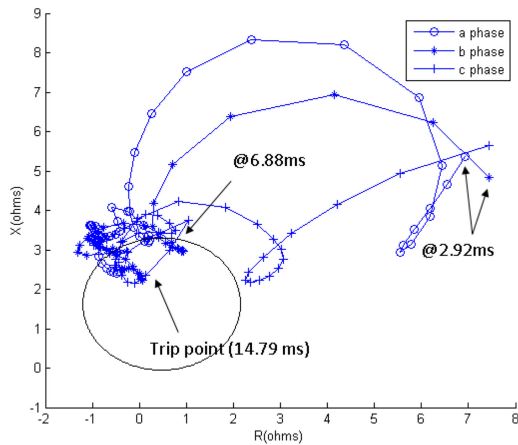


Fig. 27 Impedance trajectory of abc-to-g fault at 480 km (80% of the transmission line)

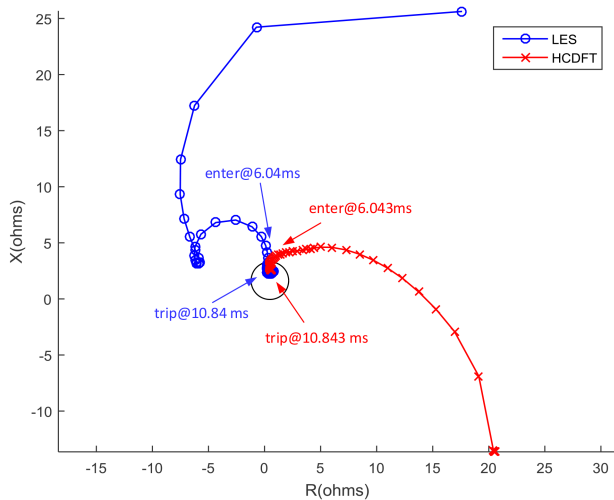


Fig. 28 Impedance trajectory for an a-g fault at 384 km (64% of the transmission line) (HCDFT versus LES results)

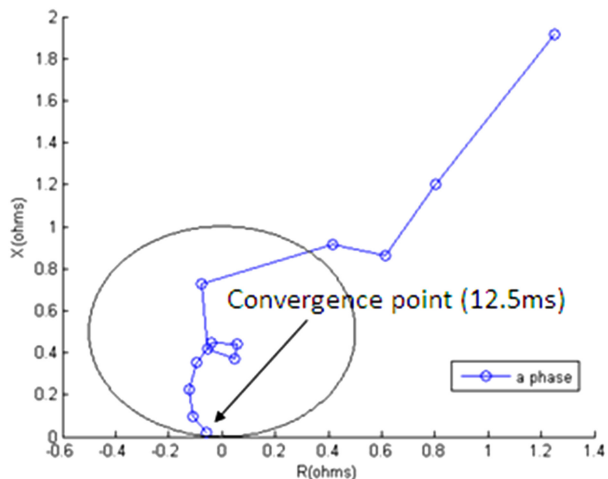


Fig. 29 Test results with an Actual COMTRADE Fault Data from a 138 kV system (a-g fault)

4.3 COMTRADE data testing with an actual fault event on a 138 kV line

Fig. 29 shows the results with the LES method with an actual COMTRADE fault event data for a 138 kV system. The fault happens right at the breaker location. The 21 distance function tripped for this scenario. The results of the LES method are shown in Fig. 29 (the LES convergence time is 12.5 ms (0.75 cycles)).

5 Conclusions

The LES-based distance relaying is improved by adjusting the length of the estimation window and raising the sampling rate. The scheme, including a communication module is implemented on an FPGA board and is tested using PSCAD/EMTDC simulator and COMTRADE 99 communication protocols to achieve similar performance to the current sub-cycle methods in the literature. The experimental results show that the proposed relay can make a secure trip in 0.49–0.78 cycles for different faults types and locations. For faults at the boundary, the relay can trip correctly but the trip times could be larger. Also, even with extremely large CCVT transient errors, the proposed relay could make a secure trip decision.

6 Acknowledgment

The authors thank Dr. M.S. Sachdev (Professor Emeritus) for providing his lecture notes and the work he carried out on the LES method in the 1990's. The authors also like to thank Dr. Eli Pajuelo (former Ph.D. student) for providing his inputs on the sub-cycle relaying technologies and methods available in the industry.

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